CHARGE-COUPLED SCANNED IR IMAGING SENSORS

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A program is in progress directed toward showing the feasibility of infrared sensitive charge-coupled imagers by constructing imaging arrays. The detectors are of both the Schottky-barrier type and the photoconductive type. The first device objective is a 64 × 1 array of palladium silicide on p-silicon Schottky-barrier diodes that couple into a three-phase CCD shift-register. Sensitivity is expected in the 2- to 3-μm region. Barriers produced with other metals can detect radiation in the 3- to 5-μm

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window useful for thermal imaging. New ideas are incorporated into the design so that the CCD does not have to handle the background signal even if frame comparison should be necessary. Test Schottky barriers have been made to permit measurement of sensitivity and dark current. Custom-designed circuitry has been built to provide the complex pulse waveforms required for the 64 × 1 array. The masks for this array have been received, and wafer processing has been scheduled. Chemically deposited PbS and sputtered PbTe are possible detector materials of the photoconductive type. PbS, either as a photoconductor or as a PbS-Si heterojunction, has been shown to have sufficiently low dark current if cooled. Response extending to 4 μm, with peak responsivity near 10^6 V/W, has been achieved with high-resistivity photoconductive PbS. A method of delineating PbS films to give the required element size and density for the device is being developed. Sputtered PbTe, although having high photoconductive responsivity, has not yet been obtained in a form of sufficiently high resistivity.

PREFACE

This Semiannual Technical Report was prepared by RCA Laboratories, Princeton, NJ, under Contract F19628-73-C-0282 and ARPA Order No. 2444. It describes work performed from 29 June 1973 to 28 December 1973, largely in the Materials Research Laboratory and the Electro-Optics Laboratory. E. S. Kohn and M. L. Schultz are the principal investigators. K. H. Zaininger and H. Kressel are the respective Project Supervisors. Other members of the Technical Staff who participated in the research are: C. Corsi, R. V. D'Aiello, W. A. Hicinbothem, Jr., S. O. Graham, and G. Fryszman. Sven Roosild and Freeman Shepherd are the AFCRL Contract Monitors.

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I. INTRODUCTION

The purpose of this program is to demonstrate the feasibility of using charge-coupled arrays for sensing images in the infrared. An important use for such arrays is the observation of scenes by their own thermal radiation. Devices which accomplish this are already in existence and, in many cases, perform close to their theoretical limits. These devices (FLIR's)* use linear arrays of cooled IR detectors with mechanical scanning. The device proposed here is cheaper, smaller, less subject to failure due to mechanical difficulties, and, because it has frame storage, it outperforms, in principle, all existing devices. It has the advantage of vidicon-type operation while avoiding the problems of insufficient beam current density and insufficient target capacitance that have, up to now, hampered vidicons for thermal imaging. Furthermore, the potential exists for doing frame subtraction within the charge-coupled registers, so that the effects of detector nonuniformities on the large thermal background are eliminated from the signal even before it is coupled out of the wafer. We have already fabricated and tested charge-coupled visible-image sensors with resolution as high as 128 × 160. The pictures are of excellent quality, and the performance data indicate that there should be no problem extending this performance to full TV resolution. Such sensors are sensitive to wavelengths as long as 1.1 μm, the bandgap of silicon. For IR detection, another material is required. Whereas, in principle, the entire device could be made of a material such as InSb, the technological problems involved are enormous at this time. Therefore, we have undertaken to make the charge-coupled sensor out of silicon using procedures already developed but to keep the photodetectors separate from the charge-coupled registers. An attractive type of photodetector for this application is the Schottky-barrier detector consisting of metal electrodes deposited directly on the silicon wafer along each row of charge-coupled registers. Schottky-barrier photodetectors have received considerable attention recently with the development of devices having quantum efficiencies as high as a few percent.** The selection of the metal and the

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*FLIR - Forward Looking Infrared Radar.
**Private communication by A. Yang.

silicon polarity provides a wide choice of cut-off wavelength and cooling requirements. In order for Schottky-barrier detectors to be compatible with CCD's, the majority carriers injected over the Schottky barrier must be converted to minority carriers for transfer to the charge-coupled registers. A scheme for doing this was proposed to RCA by Air Force Cambridge Research Laboratories,* and involved field-effect transistors fabricated at the same time as the charge-coupled registers. We are fabricating a 64 x 1 linear array of Schottky-barrier detectors scanned by a charge-coupled register. This is considerably larger than the 20 x 1 array originally proposed. The detectors are Pd on p-silicon, a type already demonstrated to be useful in the 1- to 3-μm region. Such an array can "see" moderately warm objects by their thermal radiation and, if desired, can be scanned mechanically in the second direction to demonstrate two-dimensional imaging, though without the advantage of frame storage.

A program to evaluate polycrystalline PbS films as the detectors is also under way. It is well known that the quality of such films is less than those of single-crystal material. However, because the final structure we are proposing is a frame storage device, reduction in quantum efficiency by a factor of 100 or so will not drop the performance below that of present-day FLIR's. The use of CCD scanning of area sensors makes possible the utilization of technologies whose performance had previously been considered too poor to be interesting.

*Private communication by S. Roosild and F. Shepherd.

II. OPERATION OF CCD WITH SCHOTTKY-BARRIER DETECTORS

A diagram of the structure is shown in Figs. 1 and 2. These figures represent a proprietary improvement by RCA over a Schottky-barrier CCD with MOS transfer originally proposed by AFCRL in September 1972. An n^+ diffusion at the left of each illustation is biased to $+V_o$ and is used as a charging bus. When the charging gate receives a positive clock pulse, each Schottky barrier becomes biased to V_1. After the charging clock pulse ends, the potential profile for conduction band electrons is as shown in curve (a). After exposure to the photon flux for a frame time, the Schottky barrier is discharged to curve (b) if only background is present or to (c) if signal is also present. The application of a positive clock pulse V_T to the transfer gate results in the barrier under the gate dropping to V_T'.

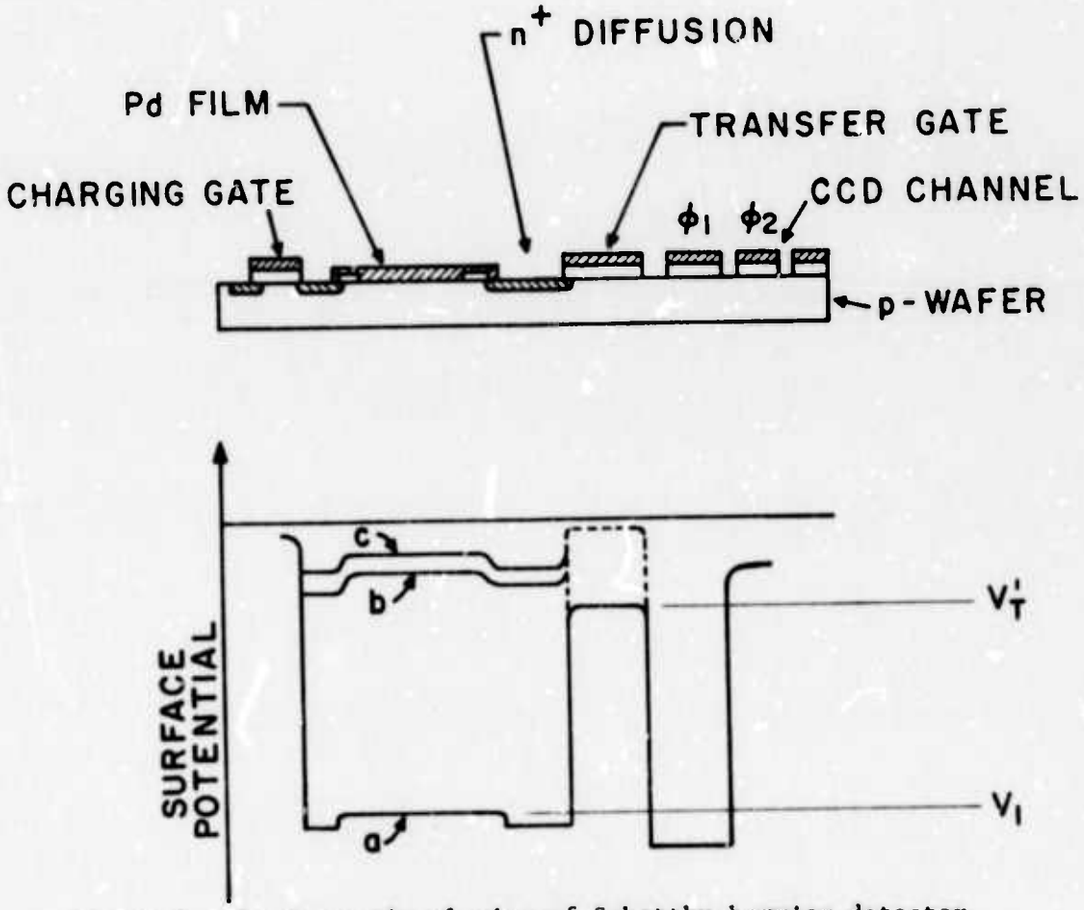

Figure 1. Cross-sectional view of Schottky-barrier detector coupled to a CCD channel by means of a transfer gate. Below is shown the surface potential as a function of position for the three conditions discussed in the text.

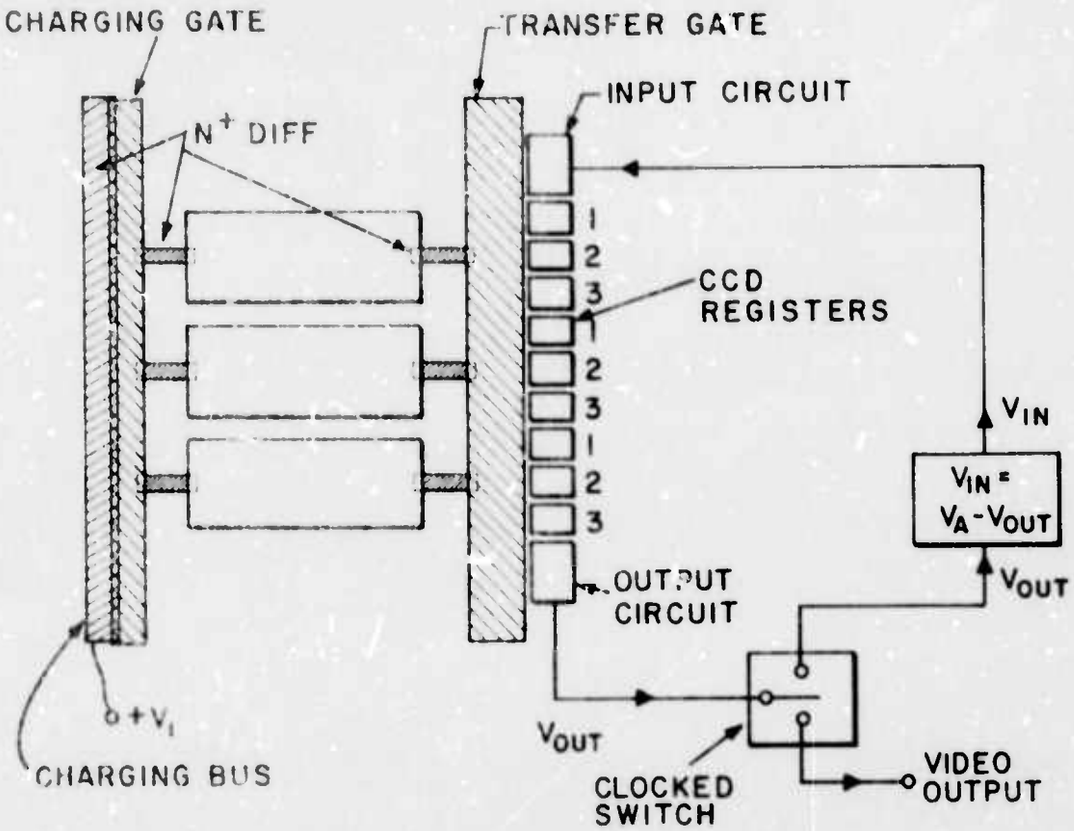

Figure 2. Top view of a Schottky-barrier array coupled to a CCD register. A circuit is shown illustrating frame subtraction.

Electrons now flow from the Pd film through the n^+ transfer diffusion, through the induced channel under the transfer gate, into the neighboring CCD register. The current continues until the Schottky barrier is charged below V_T'. Thus, the charge transferred to the register is the number of photoexcited holes less an adjustable constant. If reasonable uniformity can be obtained with the Schottky-barrier detectors, V_T' can be set to eliminate most of the background charge from the thermal scene before it reaches the CCD register, thus improving the contrast and substantially reducing the amount of charge that the CCD register must handle. This concept of operation of CCD devices has an extremely important advantage in that the bulk of the background signal is never processed by the CCD or in subsequent cancellations, a feature that makes IR-CCD's more practical by reducing to manipulatable levels the large signals normally encountered in thermal infrared sensors.

V_1 is chosen so that the Schottky barrier discharges to a few volts of reverse bias after exposure to the scene. The CCD gates must have enough capacitance so that, with the applied voltage, they can store the charge without the surface potential dropping below V_T'. This condition is easy to satisfy if most of the background is blocked as described above.

If this condition is satisfied, <u>all</u> of the photogenerated charge above transfer threshold is coupled to the CCD register. There is no capacitive division. The CCD capacitance need not be large compared with anything else. After the transfer pulse is over, the charges are passed along the CCD register, and a video signal with enhanced contrast is coupled out. While the charges are being transferred out, the transfer gate is clocked off, so there is no picture smear.

III. THE NEED FOR FRAME SUBTRACTION

The need for signal processing in a thermal viewing camera arises because of the large background. A typical requirement for a thermal viewer is to be able to recognize an object at 300.1°K in a uniform 300°K scene. In this case, the "signal" is the difference between the number of photons arriving from the hotter object and the number arriving from an equal solid angle of the background. This signal can be less than 1% of the background, but, in order to see it, the sensor must read the entire background. It is this requirement of handling the entire background that taxes the target storage and beam density capability of standard vidicons and makes the solid-state alternative so attractive. But, regardless of the capability of the detector to handle the background without saturating, the presence of the background severely aggravates the problem of detector nonuniformity. If the detectors vary in sensitivity by just a few percent, the nonuniformities in the picture due to the background would overwhelm the signal which is less than 1% of the background. Detector nonuniformity is not a problem for visible detectors because of the high contrast usually present in the reflected light from visible scenes, but it is always a major consideration for thermal images. This is why, in FLIR's, the separate amplifiers for the 100 or more detectors in the linear array must be individually trimmed to compensate for differences in the detectors. However, in our proposed CCD IR image sensor, it is neither desirable nor necessary to adjust the gains of the individual detectors. If the detector sensitivities are not sufficiently uniform, a much better method is available, namely frame comparison. If the video signal corresponding to a scene is compared with an artificial uniform scene, the effect of detector nonuniformity on the large background can be subtracted out. The artificial uniform scene can be a shutter or chopper wheel that is closed on alternate frames. A new method under consideration involves the use of an electrically switched liquid-crystal window to eliminate moving parts entirely. We have already developed and demonstrated an image comparison thermal viewer using a silicon storage tube with a pyroelectric vidicon, clearly displaying the benefits of image comparison. The advantage of doing this with a CCD detector is that the comparison can be done in the CCD register itself so that external signal processing is not required.

It should be remembered that there are important applications for which frame comparison is not required. High contrast targets such as jet plumes can be observed in the 2- to 3-μm range with a detector array of moderate uniformity without frame comparison. For such a scene, the setting gate need not be used. The transfer gate resets the detector, and the charge so transferred is proportional to the photosignal.

IV. FRAME SUBTRACTION IN A LINEAR CCD REGISTER

A CCD register can be provided with an input circuit as well as an output circuit, as illustrated in Fig. 2. After the Schottky-barrier detectors are set, they are exposed to a uniform shutter for a frame time after which a charge corresponding to the number of photoelectrons (or holes) at each barrier is transferred to the neighboring CCD gate by action of the transfer gate. This charge is actually proportional to the photosignal minus a constant dependent on the transfer voltage. The CCD register is then clocked bringing out a signal proportional to each charge. For frame comparison, we subtract this signal voltage from a larger constant voltage and insert a charge proportional to the difference voltage back into the first register. After the correct number of clock pulses has been completed, each CCD element will hold a charge equal to a constant minus the original charge. This was completed in a line retrace time. The detectors are then exposed to the scene for a frame time with the shutter open. The transfer gate is again pulsed, transferring this charge to the CCD register, after which the charge in each register is proportional to a constant plus the number of scene photons minus the number of background (shutter) photons. All that remains is to clock out the difference signal and subtract the constant voltage. Every other frame can be displayed on a CRT. An electronic switch, clocked in synchronism with the transfer clock and the CCD register clock, switches the CCD output between the video output terminal and the voltage inverter on alternate frames. Thus, while the detectors may vary in sensitivity by a few percent, the effect of this variation on the large background is completely removed. The ability to do this signal processing within the CCD wafer gives the CCD IR detector a strong advantage over other IR imaging arrays.

V. PHOTOCONDUCTIVE CCD SCANNED SENSORS

Another possibility for IR image sensing involves the use of IR photoconductors such as lead sulfide. A possible arrangement is shown in Fig. 3. The photoconductor is deposited over an insulator making contact with a charging bus and a diffusion bus. External contact is made to the charging bus. The invidual transfer diffusions are large in area, extending under the photoconductor and insulator so as to have large capacitance.

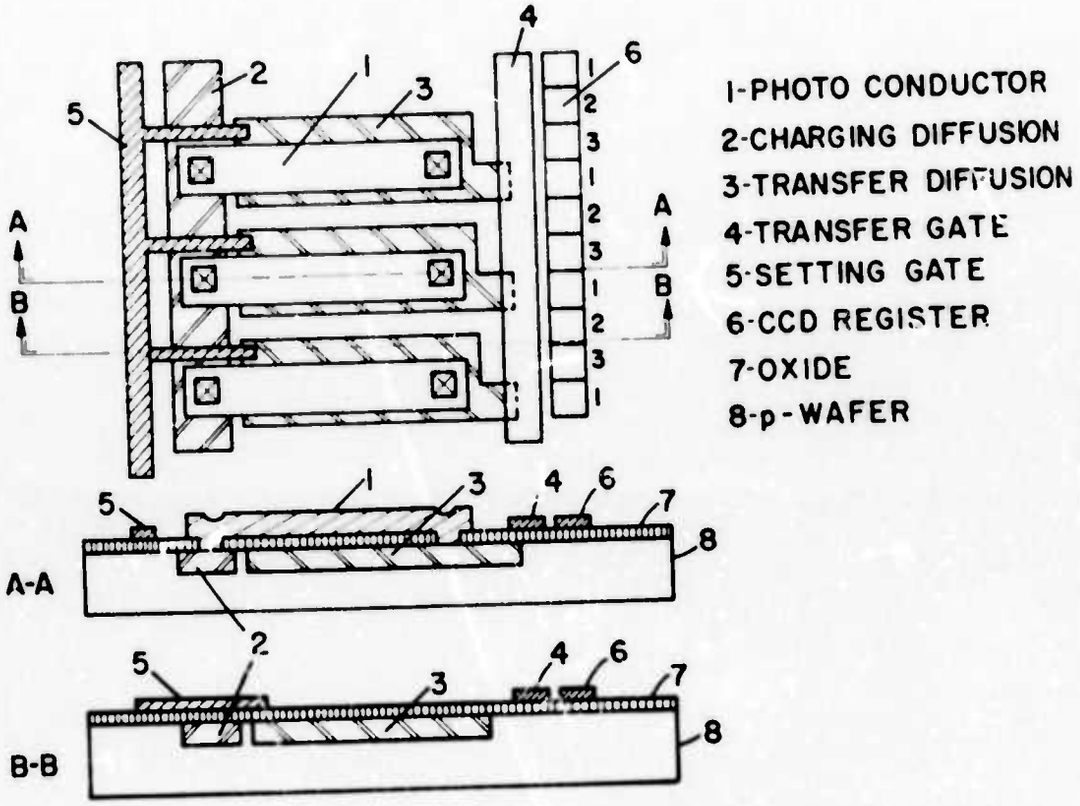

Figure 3. Top and cross-sectional views of a photoconductor array coupled to a CCD register.

The device is operated in a "see-saw" fashion so that a background signal charges the diffusions in one direction during one frame, and then, by reversing the bias on the charging bus, the scene charges the diffusions in the other direction. In this manner, the background signal is never transferred to the CCD register. However, it is important that the sensors be very uniform (to about 1%) in order for this procedure to be effective. A frame-to-frame cancellation using inverted polarity may always be used as was described for the Schottky-barrier device. Such a scheme increases the tolerable nonuniformities somewhat, but at the expense of additional complexity. The operation of the "see-saw" photoconductive detector is described below using numbers for clarity.

The charging bus is set to +20 V, and the transfer diffusions are left at +10 V after the last transfer. The photoconductors are then exposed to a uniform shutter for a frame time, charging the transfer diffusions to e.g., 15 V. The charging bus is then set to a lower potential (V_2) such as 5 V, and the shutter is opened. If the intensity of the light on a detector is more than from the shutter, it may discharge the transfer diffusion by 6 V, for example, to 9 V. We then set the transfer gate to skim the transfer diffusion to 10 V, transferring the excess charge (in this case, 1 V) to the CCD. The CCD has smaller capacitance, so that the signal voltage will be larger there, say, 10 V. The second voltage, V_2, applied to the charging bus is selected so that the initial potential drop across the photoconductor is the same before each frame; in this example, 10 V. This is important since the current through a photoconductor depends upon the voltage across it as well as on the illumination. For this method to work, it is necessary for the photoconductor to be linear and symmetrical.

The see-saw method described above is just one approach to the problem of integrating PbS type infrared photodetectors with CCD's. Another approach is to use PbS to make a heterojunction with silicon. The heterojunction can be reverse-biased as in Figs. 1 and 2 with a PbS film substituted for the Schottky barrier. Operation proceeds as described for the Schottky-barrier device. The infrared light is transmitted, as before, through the silicon, and is absorbed in the PbS film where it creates minority carriers and discharges the diode. It is not yet clear which scheme is to be preferred for making a photoconductive CCD.

VI. SCHOTTKY-BARRIER DETECTORS

Metal-semiconductor junctions have long been known as infrared detectors, but very little use has been made of the effect because of the low quantum efficiency [1]. However, recent work on palladium silicide Schottky-barrier detectors has resulted in quantum efficiencies greater than one percent.* This is high enough to be interesting in a device having frame storage. One advantage of the Schottky-barrier detector is that the cutoff photon energy is determined by the barrier height rather than by the semiconductor bandgap. Thus, the detector characteristics can be optimized for a particular application by the choice of metal even if the choice of semiconductor is limited to silicon because of the other devices on the wafer. A second advantage is the uniformity obtainable.** Since we are concerned only with the response to infrared light of photon energy smaller than the bandgap of silicon, the detection mechanism is photoemission of electrons (or holes) from the metal, over the barrier, into the semiconductor. The minority carrier lifetime (or diffusion length) in the silicon has no influence on the process, eliminating a major source of nonuniformity in semiconductor detectors. The variation in doping has little effect for similar reasons. The metal thickness does influence the quantum efficiency of the detectors when the metal film is thin, but when it is thick, and the detector illumination is through the silicon substrate as in our device, even the variations in the metal film thickness become unimportant. Thus, an array of Schottky-barrier detectors fabricated on a wafer is potentially much more uniform in response than other types of semiconductor detectors and is probably limited in uniformity only by the accuracy of the photolithographic process by which the boundaries of the detectors are defined. There is experimental evidence that this is so.** For the reasons discussed previously, this uniformity is very important for thermal images. The benefit will be lost, however, if the dark current is large and variable among detectors in the array. The dark current of an infrared-sensitive theoretical Schottky-barrier detector is due almost

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1. S. Sze, Physics of Semiconductor Devices, (Wiley-Interscience, New York, 1969).

* Private communication by A. Yang.

** Private communication by B. Capone.

entirely to internal thermionic emission of carriers from the metal over the barrier into the semiconductor. The current density for this process is given by [1]

$$J = AT^2 \exp - \left(\frac{qV_b}{kT}\right) \tag{1}$$

where A is about 100 $A/cm^2(°K)^2$, V_b is the barrier height, q is the electronic charge, k is Boltzmann's constant, and T is the temperature. With V_b equal to 0.35 eV for a palladium silicide barrier operated at 77°K, the current density is 7.7×10^{-18} A/cm^2. At 300°K it would be 11.9 A/cm^2. This must be compared with the charge storage capability of the CCD. The area of the Schottky barrier in our design is 4.5 $mils^2$ while the area of the CCD gate is 2.5 $mils^2$. The capacitance of the gate oxide is 0.1 $pF/mil^2 = 10^{-13}$ F/mil^2. Thus, the capacitance of our gate is 0.25×10^{-12} F. The charge that would cause the surface potential under the CCD gate oxide to change by 1 V is 0.25×10^{-12} F × 1 V = 0.25×10^{-12} C. If the frame time is 1/30 second, the dark current at the Schottky barrier needed to produce this charge is 0.25×10^{-12} C/(1/30) sec = 7.5×10^{-12} A. Thus, the current corresponds to a current density at the Schottky barrier of 7.5×10^{-12} A/4.5 $mils^2$ = 7.5×10^{-12} A/2.8×10^{-5} cm^2 = 2.7×10^{-7} A/cm^2. Since a 1-V swing at the CCD interface is about the maximum tolerable amount for dark signal, we take 0.3×10^{-7} A/cm^2 as the maximum tolerable, dark-current density at the Schottky barrier. Thus, it is clear that our device cannot possibly operate at room temperature. At 77°K, the calculated dark current is below the maximum tolerable amount by a factor of more than 10^{10}. This would be wonderful if thermionic emission were the only source. Unfortunately, other sources of dark current exist. One important source involves field concentration at the edge of the device. This mechanism is difficult to account for analytically as it probably involves barrier-lowering field emission and avalanche multiplication as well as other effects, all occurring simultaneously in an uncertain geometry. The result is that the reverse current increases rapidly with bias at just a few volts of reverse bias. This is shown in Fig. 4. A technique that has been successfully used to eliminate edge leakage in experimental devices is the inclusion of a diffused guard ring[2].

2. J. M. Andrews and M. P. Lepselter, Solid-State Electron. 13, 1011 (1970).

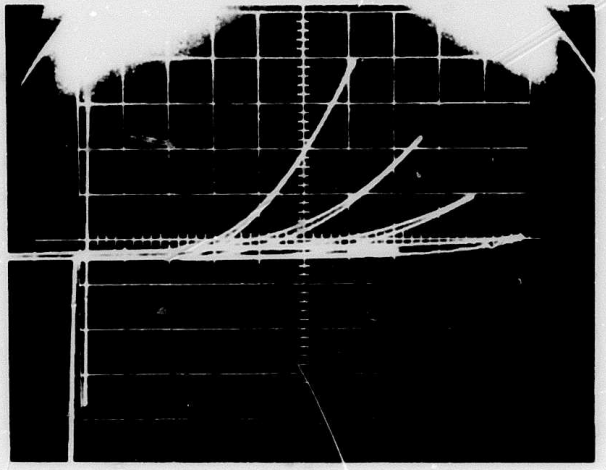

Figure 4. I-V curve of a set of palladium silicide Schottky barriers at 77°K showing edge effect in the reverse characteristic. The reverse current averaged over the area is on the order of 30 mA/cm^2 at 5 V. The four barriers shown have areas of 5.8×10^{-4} cm^2, 2×10^{-4} cm^2, 0.9×10^{-4} cm^2, and 0.2×10^{-4} cm^2. Horizontal: 1 V/div, vertical: 0.01 mA/div.

The original Schottky barrier is shown in Fig. 5(a); the same structure is shown in Fig. 5(b) except that a diffused guard ring has been added. Since the diffusion extends a few micrometers into the silicon wafer and does not end abruptly, there is much less field concentration here than at the sharp, abrupt edge of the metal-silicon interface shown in Fig. 5(a). Thus, the reverse breakdown voltage of the p-n junction can be quite high, and the presence of the guard ring eliminates the edge effects of the metal. Whereas a test device with a diffused guard ring might pin down the cause of our leakage, it may <u>not</u> be practical to incorporate this idea into a CCD because of the large diffusion area as compared with the small remaining Schottky-barrier area. In any case, we would require a new mask set to build guard rings into our CCD chip.

Another important source of dark current in a Schottky-barrier device involves surface inversion[3]. If the surface under the oxide is inverted, as it is in an n-channel (p-substrate) MOS device, the dark current measured at

3. A. Y. C. Yu and E. H. Snow, J. Appl. Phys. <u>39</u>, 3008 (1968).

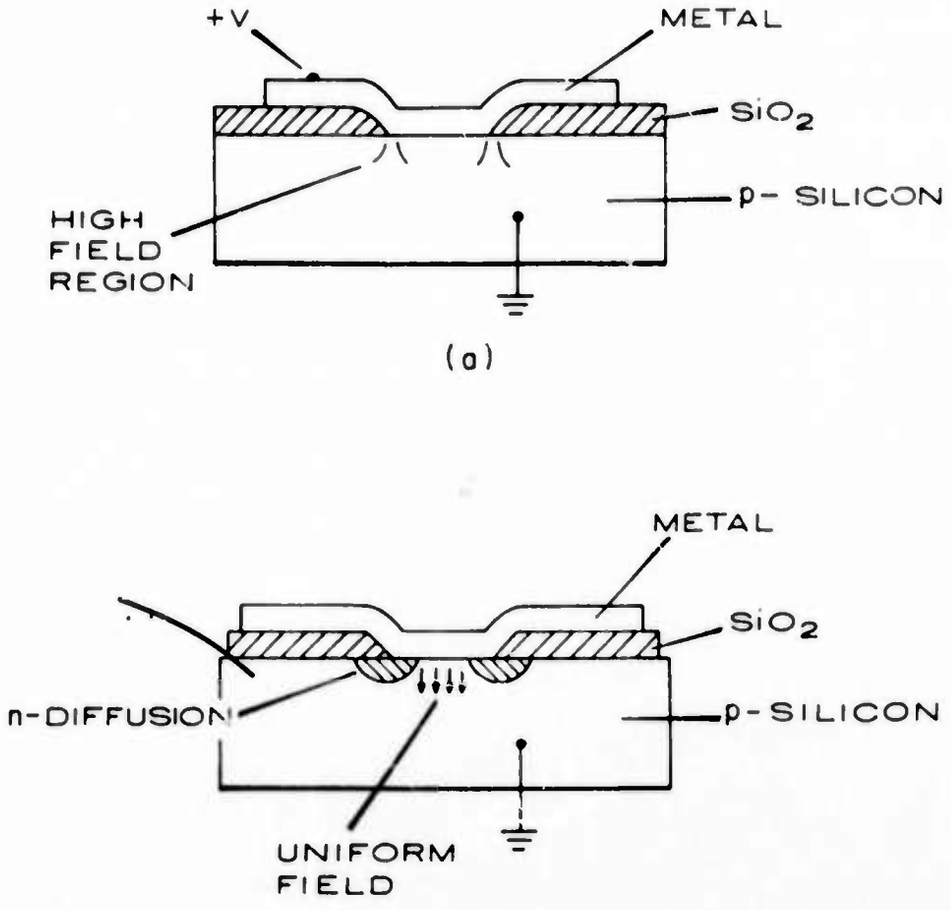

Figure 5. Schottky-barrier detectors: (a) without guard rings and (b) with guard rings.

the Schottky barrier can include the dark current of the p-n junction associated with the inversion layer. The junction can cover a much larger area than the Schottky barrier itself. This type of leakage can be pinched off with a channel stop diffusion or with a field plate biased to bring the surface beneath it into accumulation. In our IR-CCD, the Schottky barriers are surrounded on two sides by channel stop diffusion and on the other two sides by field plates, effectively eliminating this mechanism of dark current.

The starting material for our Schottky-barrier detectors was (100)-oriented p-type silicon doped to $10^{15}/cm^3$. A thermal oxide was grown, and holes were opened in the oxide ranging in diameter from 2 mils to 10 mils. Palladium was evaporated in a sodium-free vacuum system while the silicon wafer was heated to permit the reaction forming palladium silicide. The unreacted palladium

was removed with an etch, and gold was evaporated and defined to form contacts to the silicide. The chips were mounted with epoxy in IC flatpacks, each over a hole to permit rear illumination. Several diode contacts were bonded in each flatpack. The devices were tested for spectral sensitivity and dark current at 77°K. A typical relative spectral response curve is shown in Fig. 6. The peak at 0.9 μm is caused by absorption of light in the silicon substrate and collection of the minority carrier photoelectrons by the barrier. The peak response is estimated at a few percent quantum efficiency. The response beyond 1.1 μm is clearly due to absorption in the metal film and photoemission of holes from the metal to the silicon. Its quantum efficiency is down from that of the peak silicon by a factor of 2 near the silicon band edge to 10^3 at 2.8 μm. Thus, the best quantum efficiency seen here for the barrier in the IR mode is about 1%. The reverse current typical of our best Schottky barriers so far is about 30 mA/cm^2, four orders of magnitude too high, at 5 V. This is seen in Fig. 4. Thus, unless a substantial improvement can be obtained, the dynamic range of our device will be only a few volts. It is not clear whether this is sufficient for device operation.

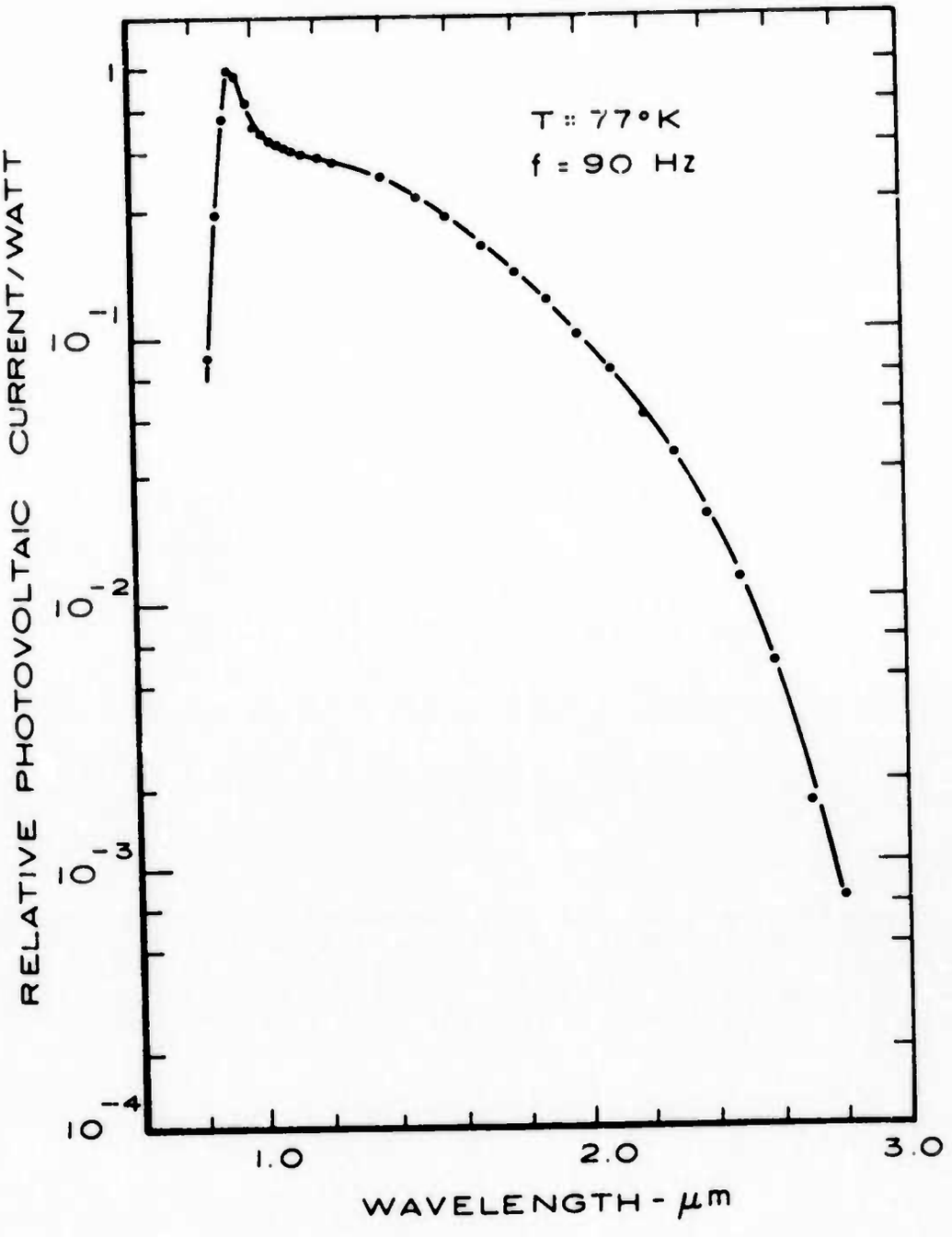

Figure 6. Relative spectral response of Schottky-barrier detector. The material was palladium-silicide on p-type silicon at 77°K.

VII. DESIGN OF THE INFRARED CCD

Charge-coupled semiconductor devices [4] consist of closely spaced MOS capacitors pulsed into deep depletion by the clock phase voltages. For times much shorter than that required to form an inversion layer of minority carriers by thermal generation, potential wells will be formed at the silicon surface. The minority-carrier charge representing the information will be stored or confined in these potential wells. The propagation of the information is accomplished by clock pulses applied to the electrodes of the successive MOS capacitors (i.e., charge-coupled elements) which results in a motion, or spilling, of charges from the potential wells that are becoming shallower to the potential wells that are becoming deeper. Such propagation of signal into the successive minima of the surface potential produces a shift-register for analog signals having signal transfer efficiency approaching unity. The simplest structure that accomplishes this is shown in Fig. 7(a).

If the charge-coupled structures are formed with symmetrical potential wells, at least three clock phases are required to determine the directionality of the signal flow. One interesting feature of the three-phase system is that it may be used for a bidirectional charge-coupled channel in which the flow of information may be reversed by reversing the timing of the two phase clocks.

Two-phase operation is also possible but it requires the charge-coupled structures to be formed so that the potential wells induced by the phase voltage pulses are deeper in the direction of the signal flow. In this case, as one phase voltage is lowered, the resulting potential barriers force a unidirectional signal flow. This can be accomplished with the structure in Fig. 7(b) if adjacent pairs of aluminum and polysilicon electrodes are connected together and alternate pairs are connected to the two clock phases. The signal charges reside under the polysilicon gates where the oxide is thinner and the potential well deeper, and transfer upon clocking to the adjacent pair. It is possible to operate this device with a single clock phase if a proper dc voltage is applied to one of the phases.

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4. W. S. Boyle and G. E. Smith, Bell Syst. Tech. J. 49, 587 (1970).

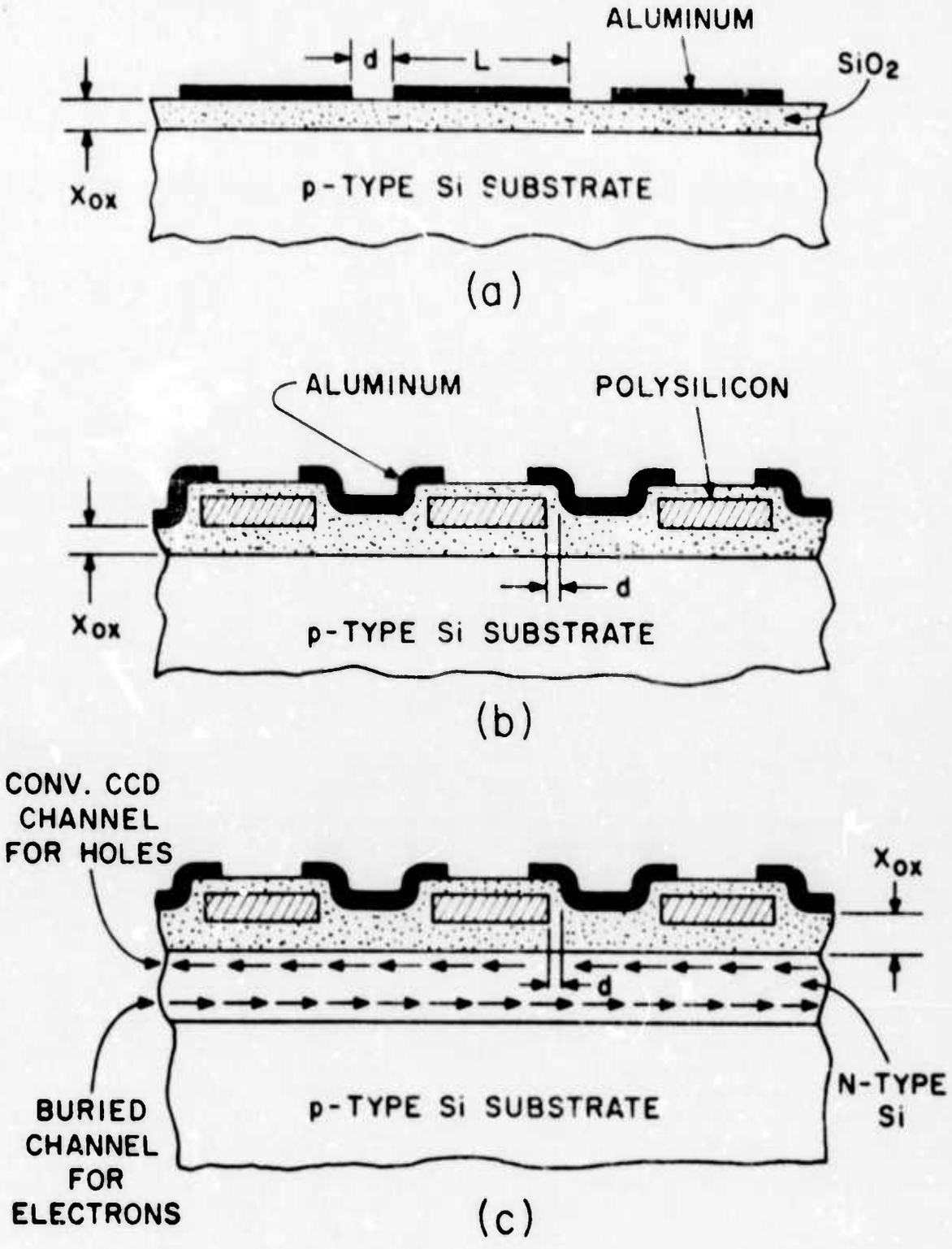

Figure 7. Three types of charge-coupled structures: (a) single-metal CCD's, (b) sealed-channel CCD's in the form of polysilicon gates overlapped by aluminum gates, and (c) buried-channel CCD's.

In CCD operation the signal charge must be confined to a narrow potential well called the channel. This channel should provide a deep, abrupt potential well that changes surface potential in response to the clock pulse voltages. The region outside the channel should be insensitive to clock voltage changes and should be in accumulation.

There are three general methods for channel confinement presently being investigated at RCA Laboratories: (1) two thicknesses of oxide or thick field oxide, (2) guard ring diffusion or "channel stops," and (3) electrostatic guard rings in the form of polysilicon layers.

The two-oxide method operates by creating a deeper potential well under the thin oxide than under the thick oxide. It works best on low-resistivity substrates. A problem that sometime occurs, however, involves metal continuity over the oxide step.

Our present choice of channel confinement for area CCD's is to use diffused guard rings as channel stops. This approach is applicable to high-resistivity substrates and also provides for the simplest processing for large-area CCD's. Ideally, the diffusion channel stops should be very abrupt and relatively low doped (10^{17} to $10^{18}/cm^3$).

The important difference between the first two methods of channel confinement and the polysilicon electrostatic guard rings, also referred to as polysilicon field shield, is that in the latter case the surface potential at the channel stop can be determined by an externally controlled potential. Thus, the regions between the CCD channels can be accumulated or held at any other surface potential. This capability may be useful in the operation of the CCD but at the cost of greater fabrication complexity.

The following three charge-coupled structures are available for the construction of CCD arrays: (1) single metal CCD's, (2) sealed-channel two-phase or multi-phase CCD's, and (3) buried-channel CCD's. The cross-sectional views for these three charge-coupled structures are illustrated in Fig. 7. The comparative merits and trade-offs of the three above-mentioned charge-coupled structures are discussed below.

Single-metal-layer three-phase charge-coupled devices made in a p-MOS or a n-MOS process require the minimum number of processing steps. The most conventional process and the one used to make the first charge-coupled circuits at RCA is the thick-oxide p-MOS process. The major limitation

of this process is the etching of the separation between the gates; it should be no larger than about 2.0 μm to control the surface potential in the resulting gap in the channel oxide. The operation of n-MOS CCD's, on the other hand, can be less sensitive to the interelectrode spacings because of the presence of positive charge in the channel oxide. CCD's in the form of n-channel structures using single metallization, diffusion guard rings for the channel confinement, and only a single thickness of oxide are the simplest to fabricate. We therefore adopted this approach.

The sealed-channel polysilicon-aluminum structures developed at RCA Laboratories [5] and shown in Fig. 7(b) are the most compact structures that can be fabricated with more or less conventional layout rules. The self-aligning-gate construction of these devices allows fabrication of charge-coupled structures with gate separation comparable to the thickness of the channel oxides as well as having the channel oxide always covered by one of the metallizations. Another important advantage of the silicon-gate process is that it provides a very simple method for the construction of two-phase CCD's. Charge transfer efficiencies of 99.99% per stage have been obtained in the operation of such p-channel two-phase CCD's operating at clock rates up to 2 MHz. This we believe is the highest charge transfer efficiency reported thus far in the operation of conventional CCD structures. We chose not to use this method at this time because our 64 × 1 array does not need the extra bit of transfer efficiency to warrant the additional complexity of fabrication.

The buried-channel CCD [6] represents a charge-coupled structure in which the potential minimum for the charge signal is located inside the silicon substrate about 0.5 to 1.0 μm below the SiO_2-Si interface. The buried channel structure is illustrated in Fig. 7(c). The completely depleted n-type layer forms a parabolic potential variation which, for a wide range of gate voltages, results in a potential minimum for electrons near the center of the buried-channel layer. This layer can be initially depleted and maintained in depletion by charge transfer action. Since the

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5. W. F. Kosonocky and J. E. Carnes, "Two-Phase Charge-Coupled Device," Final Report, Contract No. NAS1-10983, February 1972.
6. R. H. Walden et al., Bell Syst. Tech. J. 51, 1635 (1972).

carriers are a distance from the surface, they avoid surface state trapping, and thus the bias charge (or fat zero) required for efficient surface channel operation is not required here. However, this is not an advantage for thermal imaging where a large background is present anyway. Again, the advantage for us, if any, does not warrant the complexity.

With the choice of a single-level metallization type structure and diffused channel confinement, the fabrication procedure is as follows. A $10^{15}/cm^3$ doped (100) silicon wafer is subjected to a p-type diffusion and an n-type diffusion, each defined by a thermal oxide left after a photolithographic step. The gate oxide is grown, and contact holes are opened. Palladium is then evaporated onto the wafer in a vacuum system that received special care to avoid sodium contamination. Any sodium would get into the oxide in ionic form and cause the device characteristics to drift. While the palladium is being evaporated, the wafer is heated, causing palladium silicide to be formed in a chemical reaction. The wafer is then removed from the evaporator, and the remaining metallic palladium is etched off. It is returned to the vacuum system, where it receives a thin evaporated film of titanium followed by a film of aluminum. The titanium layer is required because aluminum reacts with palladium silicide. The aluminum is defined photolithographically with an etch that stops at the titanium. The titanium is then etched down to the gate oxide with an etch that does not attack aluminum. A protective SiO_2 layer is next deposited over everything, and holes are opened for the bonding connections. The wafers are scribed and diced, and the chips are mounted with epoxy in integrated-circuit holders with holes cut to permit rear illumination. The final step is to bond leads from the bonding pads on the chips to the holders. A summary of the fabrication procedure and mask levels is shown in Fig. 8. If this were a visible-sensing CCD, it would be necessary to thin the chips to permit rear illumination. Fortunately, this step is not necessary for us since silicon is transparent to infrared light beyond 1.1 μm.

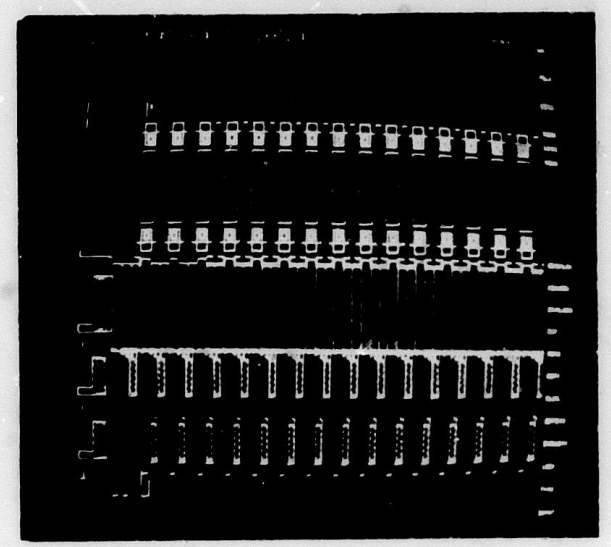
Our design is a 64 × 1 linear CCD with gates 0.52 mil long in the direction of charge transfer and 0.08-mil gaps. The repetition length is thus 1.8 mils per bit, and the channel is 5.0 mils wide. The Schottky-barrier contact holes are rectangles 5.0 mils by 0.9 mil and are spaced on

Operation Performed by	Fabrication Steps
INTEGRATED-CIRCUIT TECHNOLOGY CENTER, David Sarnoff Research Center, Princeton, NJ	1. Diffuse channel stop (Mask 1) 2. Diffuse source and drain (Mask 2) 3. Etch contact holes (Mask 3)
METALLIZATION LABORATORY, Solid-State Technology Center, Somerville, NJ	4. Clean wafer 5. Evaporate and drive in palladium 6. Remove excess palladium 7. Evaporate titanium and aluminum
INTEGRATED-CIRCUIT TECHNOLOGY CENTER, David Sarnoff Research Center, Princeton, NJ	8. Etch pattern in aluminum (Mask 4) 9. Etch titanium using aluminum as mask 10. Deposit SiO_2 overcoat 11. Etch bonding holes and scribe lines in SiO_2 (Mask 5) 12. Scribe and cleave wafer 13. Mount chip in package and bond leads

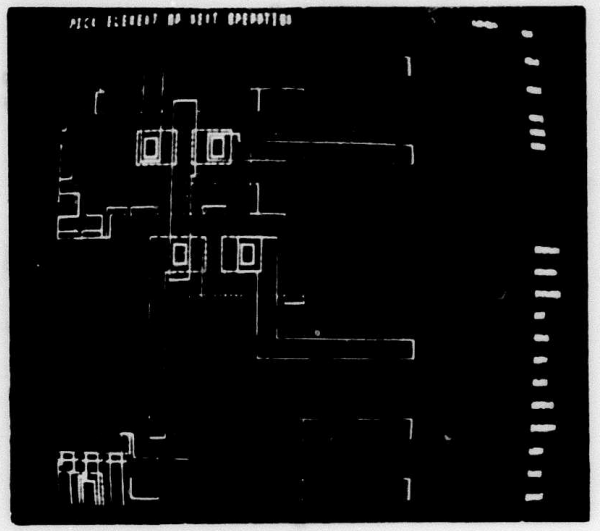
Figure 8. Procedural steps in fabrication of Schottky-barrier infrared CCD's.

1.8-mil centers along the CCD register so that each detector can load into a phase-one CCD gate when the transfer gate is clocked. There is a source diffusion with loading gates at one end of the shift register and a resettable floating diffusion connected to an on-chip MOS transistor at the other end. Numerous other devices are on the chip, including alignment marks, photolab marks, level numbers, devices for measuring metal resistivity, diffusion resistivity, diffusion lateral spread, channel stop threshold, MOSFET characteristics, etc.

The masks were drawn, programmed and punched on computer cards, and examined on a computer-generated CRT display. There, dimensions could be checked, and programming errors could be easily spotted. Photographs of the CRT display are shown in Fig. 9. Several mask levels are shown superimposed with different kinds of lines to represent the different mask levels. It was possible to zoom in to measure coordinates, and to change the sections and levels displayed very quickly. When we were satisfied that no errors remained, the punched-card program was converted to a tape, and a large flat-bed ink-plot was generated from the tape with a different color for each mask level. We scrutinized this plot for errors, and



(a)



(b)

Figure 9. Computer-generated CRT displays of sections of the chip. Four of the mask levels are shown as different kinds of lines. (a) The beginning of the CCD array. The Schottky barriers can be seen along the top row. The shift register is the center row. (b) A close-up view of the CCD output stages. The top device is the MOS output transistor. The similar device in the center is the floating diffusion with its reset gate and drain.

proceeded to order masks to be generated from the computer tape. At the time of this writing, the masks have been delivered, and the processing scheduled.

VIII. CIRCUITRY FOR THE INFRARED CCD

A three-phase charge-coupled line array without separate detectors requires three voltage waveforms consisting of overlapping pulses. Our CCD with separate detectors has additional requirements. Once in each frame time a pulse must be applied to the setting gate. A preset time after this pulse ends, a different pulse must be applied to the transfer gate. While the transfer pulse is on, the CCD pulse trains must stop with phase 1 high and phases 2 and 3 low so that the accumulated electrons can be transferred into the potential wells under the phase gates without smearing. After the transfer pulse ends, the CCD pulse train must begin again and must run long enough to drive the electrons from the first gate to the detector at the other end of the line. The next setting pulse must be applied a suitable time later to achieve the desired frame rate.

It is possible to generate the five waveforms described above using a series of one-shot flip-flops triggering each other in a suitable way, but a change as simple as varying the bit rate would require careful resetting of many adjustments. A better way is to generate the three-phase CCD waveforms using logic circuitry. A pair of cascaded flip-flops driven by a clock and wired to operate as a divide-by-three circuit has two of the three required waveforms appearing at its output terminals. The third is easily generated from these two using logic. Changing the clock rate controls the bit rate without affecting the timing relationship between the three waveforms. Thus, a design was completed in which the three-phase pulse trains are generated logically from a clock while the auxiliary pulses and time delays are generated by monostable multivibrators. The two systems are interconnected with logic to hold up the clock with phase 1 on while the transfer pulse is applied and to restart the clock after the transfer pulse ends. This design has been constructed using 12 TTL DIP packages. Five gate-driving amplifiers with variable pulse height are needed, and these have been built with complementary-symmetry bipolar transistor circuitry. A detailed discussion is presented in Appendix A.

IX. LEAD SULFIDE

A. INTRODUCTION

Photoconductors have long been used as detectors of infrared radiation. As such, they are possible sensor materials for the CCD imaging device. The two modes of operation of a CCD employing photoconductive sensors have been outlined in Section V. The photoconductor will be used as a layer on the order of 1 μm thick. This must have sufficiently large optical absorption so that the incident radiation is efficiently utilized.

The sensor material for the CCD must satisfy certain conditions that are not important for a conventional detector. If the material is used as a photoconductor, the dark resistance of the sensor element must be sufficiently large so that the element is not completely discharged by dark current within a frame time. This condition sets a lower limit to the resistivity of the material of about 2×10^6 ohm·cm if the sensitive element is 1 μm thick and has a length-to-width ratio of five. A target value, then, would be on the order of 10^7 ohm·cm. If the material is used as a heterojunction with Si, the reverse-bias leakage current must be low just as for the case of the Schottky-barrier sensor discussed earlier. In addition, the sensor material must be compatible with the Si processing technology required for fabrication of the CCD and it must be capable of being delineated, by photolithographic and etching procedures, to produce sensor elements of the required size and packing density without intolerable degradation of properties.

The CCD requirements of high resistivity for photoconductors or low reverse-bias leakage for heterojunctions are most likely to be met by polycrystalline films of the lead chalcogenides PbS, PbSe, and PbTe. These materials have long been employed as sensitive infrared detectors. Review articles describing their properties and performance are available[7-9]. Lead sulfide has been chosen for most intensive investigation in the present program since it is the lead chalcogenide most likely to be obtainable in a high-resistivity form. Its energy gap is 0.31 eV at 77°K[7] and it should, therefore, exhibit response to wavelengths as long as 4 μm.

7. R. Dalven, Infrared Phys. 9, 141 (1969).
8. D. E. Bode, Physics of Thin Films, Eds. G. Hass and R. E. Thun, Vol. 3, (Academic Press, New York, 1966), pp. 275-301.
9. T. S. Moss, Advances in Spectroscopy, Ed. H. W. Thompson, Vol. 1, (Wiley-Interscience, New York, 1959), pp. 175-213.

Lead sulfide films can be prepared by evaporation, by sputtering, and by chemical deposition. The latter method is favored for production of PbS detectors and is the one chosen for the present work. Films as prepared usually have low resistivities. Post-deposition heat treatment often leads to spectacular increases of resistivity. Mahlman[10] has shown that resistivities of chemically deposited PbS films can be as high as 10^9 ohm·cm at 100°K. His films were prepared by incorporating an oxidizing agent (identity not specified) in the deposition solution. After deposition, his films were vacuum baked at an unspecified temperature. The resistivities of the films at 100°K varied between 10^2 and 10^9 ohm·cm, depending upon the amount of oxidant used.

The major portion of the photoconductor work to date under this program has been devoted to the development of a procedure for the preparation of high-resistivity PbS photoconductor films compatible with CCD device processing. The investigation of the problem of the delineation of PbS films without degradation of their properties to provide the element size and density required for the device is under way. Some results on the properties of PbS-Si heterojunctions have been obtained. Leakage currents sufficiently small for CCD sensor use have been observed. The heterojunction mode of operation is attractive since it is basically the same as that employing the Schottky-barrier sensor.

B. PREPARATION OF PbS FILMS

There is a voluminous literature on the preparation of photoconductive PbS films by chemical deposition. No attempt will be made to review this literature at the present time. The review articles [7-9] quoted above include discussions of chemically deposited PbS and give references to some of the original literature.

The recipes given include, as common constituents all in an aqueous solution, a lead salt, $Pb(NO_3)_2$ or $Pb(C_2H_3O_2)_2$; an alkali, usually NaOH or KOH; and thiourea, $CS(NH_2)_2$. The formation of polycrystalline, mirror films of PbS occurs over wide ranges of concentration of these constituents. In addition, many recipes sometimes include small concentrations of one or more additives: oxidizing agents, metal salts, organic bases, or other organic compounds. Occasionally, the use of an additive is mentioned without its identity being specified [10,11].

10. G. W. Mahlman, Phys. Rev. 103, 1619 (1956).
11. S. Espevik, C. Wu and R. H. Bube, J. Appl. Phys. 42, 3513 (1971).

No systematic study of the effects of variations of the composition of the deposition mixture upon PbS film properties has been made during this investigation. A judicious "averaging" of the recipes given in the literature was made to provide a trial recipe. When this was found to yield reasonably sensitive photoconductive films, the recipe was used throughout the present work except in the attempts to use Al electrodes with PbS.

The films were deposited from solutions in which the constituents and their concentrations (after mixing and disregarding the reactions which occur) were

NaOH	0.4 M
$Pb(NO_3)_2$	0.033 M
Thiourea	0.15 M
H_2O_2	~0.01 M

Kunze et al. [12] have reported that the addition of small concentrations of H_2O_2 to the deposition solution increased the responsivity of the films. The solution was prepared by the addition of measured volumes of reagent solutions of known concentrations to a beaker containing the substrates, face down, in a measured volume of water. Additions were made as the solution was being gently stirred by a magnetic stirrer. Deposition, at room temperature, was usually allowed to proceed for 30 minutes. After deposition, the films were rinsed in distilled H_2O, gently swabbed with cotton, and then allowed to air dry.

Substrates were made of 1-in. × 3/8-in. polished vitreous silica plates cleaned in chromic acid or of silicon, bare for heterojunction samples or coated with SiO_2 for photoconductor samples. When it was desired to limit the area of deposition, masking was done with a painted-on solution of Apiezon Hard Wax W* in trichlorethylene (TCE). After deposition, the mask was removed from the rinsed, dried film with several rinses of warm TCE.

12. O. A. Kunze, O. G. Malan, P. A. Buger, and W. Fink, Z. Naturforsch. 26B, 8 (1971).

*Manufactured by Associated Electrical Industries, Ltd., England.

Film thicknesses were calculated from the weight of a film of known area and the bulk density of PbS. The film thicknesses ranged from 0.3 to 0.6 μm for different depositions. In a given deposition, the thickness of a film deposited on a substrate on the stirring axis differed from one deposited near the container wall by not more than about 0.02 μm. When films thicker than about 0.5 μm are desired, multiple depositions must be carried out. All of the films studied thus far have been single layer films.

C. MEASUREMENT OF FILM PROPERTIES

Electrodes used for measurement of resistance and photoresponse of the films included Ag paint applied after film deposition and evaporated Au or evaporated Ti applied to the substrate before film deposition. Several attempts to use evaporated Al electrodes were made since this metallization is commonly used in Si device technology. These were unsuccessful because (a) Al reacts with alkaline solutions and (b) Al reacts with PbS deposited over it. Electrode spacing for photoconductor samples was usually about 0.5 to 1.0 mm and the electrode width, a few millimeters. Resistivities were calculated from measured resistance values and the sample dimensions.

All electrical measurements were made with the samples mounted in the vacuum space of a small, demountable glass dewar which had a vitreous silica outer wall. The substrate was pressed, by spring clips, against a flat ground on the inner member of the dewar. Electrical connection to the film electrodes was made with 5-mil Pt wire and Ag paint. Sample temperature during cooling or during heat treatment was measured by means of a Cu-Constantan thermocouple junction soldered to a small Cu tab that was pressed against the substrate by one of the spring clips. Thermocouple and sample leads were brought out at the top of the dewar. Heat treatment of the films in vacuum ($p \sim 10^{-5}$ torr) or in room air was done by surrounding the lower part of the dewar with a small furnace.

Measurements of the temperature dependence of resistance below room temperature were made as the samples were cooled slowly by the intermittent addition of small amounts of liquid nitrogen to the dewar. The temperature

drift could be made slow enough to obtain a reasonable approximation to thermal equilibrium. When the samples had cooled, great care was exercised to shield them from stray radiation in order to obtain reliable dark resistance values.

Photoresponse was measured in the conventional manner using chopped radiation, usually at 90 Hz, from a Leiss double NaCl prism monochromator or from a 500°K blackbody source. The relative flux in the monochromator beam was determined with a radiation thermocouple. The ac signal voltage developed across a load resistor in series with the sample and a bias voltage supply was measured with a Princeton Applied Research HR8 lock-in amplifier.

Photoconductive responsivity is usually expressed in volts per watt. The value so quoted is a function of load matching conditions and of bias voltage. The responsivity can be expressed in a form that is independent of these quantities and of the sample geometry by

$$\Delta\sigma = \frac{\ell V_s}{wtV_B R_L}\left(\frac{R_C+R_L}{R_C}\right)^2 \qquad (2)$$

$\Delta\sigma$ is the change in conductivity per watt of incident radiation, V_s is the responsivity in volts per watt for the conditions of the measurement; V_B is the bias voltage; R_C is the sample resistance; R_L is the load resistance; and ℓ, w, and t are the sample length, width, and thickness, respectively. This method of expressing the responsivity is meaningful as long as V_s is proportional to V_B and R_C is independent of V_B or if $R_C \gg R_L$. Values of $\Delta\sigma$ which have been observed for the films studied in this work give, for matched load conditions and reasonable values of V_B, monochromatic peak responsivities of about 10^6 volts per watt. This is on the order of typical responsivities reported for PbS detectors. The responsivity of the PbS-Si heterojunction discussed in Section IX-F has been expressed as the short-circuit current in A/W. For purposes of comparison, responsivities for the photoconductor samples may be converted to these units by employing the expression $\left(\frac{wt}{\ell}\right)V\Delta\sigma$. For a photoconductive sensor element having a length-to-width ratio of five and a thickness of 1 μm, the responsivity in A/W is $2 \times 10^{-5}\ V\Delta\sigma$.

Taking as typical values, V = 10 volts and $\Delta\sigma = 10$ (ohm·cm·watt)$^{-1}$, the responsivity would be 2×10^{-3} A/W. However, insufficient data are as yet available to determine the limits of heterojunction sensitivity in the PbS detection range. The spectral response curves given in this report have been corrected for a small absorption in the SiO_2 window at wavelengths beyond 2.5 μm.

D. BEHAVIOR OF PbS PHOTOCONDUCTIVE FILMS

The chemically deposited PbS films, prior to any heat treatment, usually have room-temperature resistivies in the 1 to 10 ohm·cm range. These films exhibit only small increases in resistivity, to values usually in the 10 to 100 ohm·cm range, when cooled to liquid-nitrogen temperatures.

Heat treatment of the films for several hours in vacuum at temperatures near 100°C produced, with one exception that will be discussed later, substantial increases in resistivity. The room-temperature values increased by factors of 10 to 100 while the low-temperature values increased by up to about seven orders of magnitude. The results of Hall effect measurements by Espevik et al. [11] on presumably similar films indicate that this increase of resistivity is due primarily to a decrease in hole concentration and an increase in the activation energy for thermal excitation of holes. Much less important is a small decrease in mobility. The conductivity activation energy observed for our vacuum-annealed films is usually about 0.35 eV over the range from room temperature to about 200°K. Below this range, the activation energy decreases until near 100°K it is about 0.03 to 0.04 eV. If a vacuum-annealed film is exposed to air, its resistivity decreases by large factors, especially for low temperatures. The high-resistivity state can be restored by a subsequent vacuum bake. These changes are believed to be due to sorption and desorption of oxygen.

The behavior of a particular film, S7B, which illustrates these features, is summarized in Table 1 and in Fig. 10. Each curve gives the temperature dependence of resistivity measured after the treatment indicated in Table 1. The behavior of this sample demonstrates that it is possible to reach dark resistivities of 10^8 ohm·cm at temperatures well above 100°K with chemically deposited PbS films.

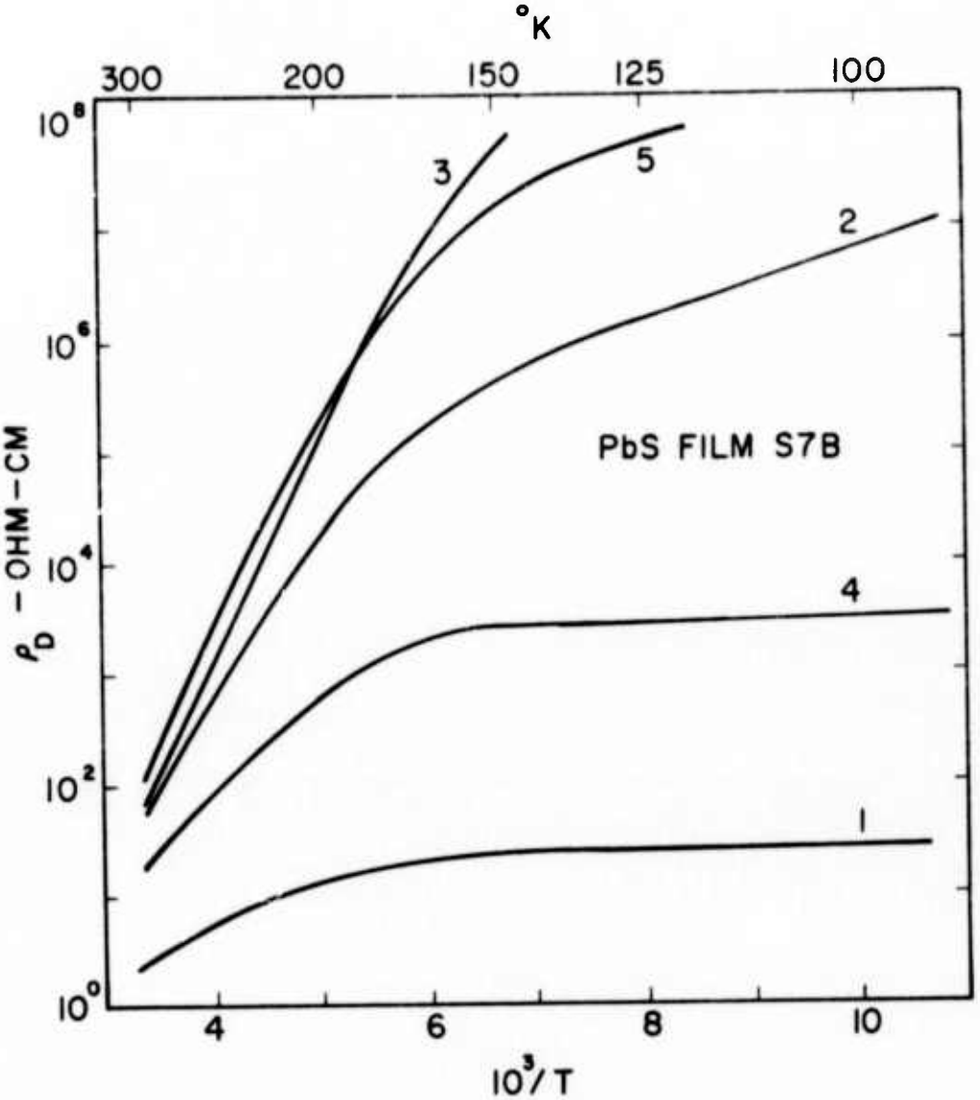


Figure 10. Temperature dependence of dark resistivity of PbS film S7B for several conditions of heat treatment.

Not all samples have shown so dramatic an increase of resistivity upon vacuum annealing as did PbS film S7B. For example, film S5B had a low-temperature resistivity of 2.4×10^4 ohm·cm after vacuum annealing for a total time of 5.5 hours at temperatures up to 130°C. Film S15C, after 3 hours at 96°C, had a low-temperature resistivity of 1.2×10^6 ohm·cm. Evidently, the vacuum annealing behavior of different films prepared in nominally the same manner can differ substantially. It is important to note, for future reference, that all did show a large increase in low-temperature resistivity upon vacuum annealing.

Table 1 - Behavior of PbS Film S7B

Curve No. (Fig. 10)	Treatment	ρ at 300°K(ohm·cm)	ρ at 100°K(ohm·cm)
1	Film as deposited	3	28
2	Vacuum anneal 2 hr at 92°C	47	8×10^{6}
3	Vacuum anneal 3 hr additional at 92°C	61	$>10^{8}$
4	Exposed to room air for 25 hr	19	3.2×10^{3}
5	Vacuum anneal 3 hr at 100°C	1.1×10^{2}	$>10^{8}$

After film S5B had reached the state indicated above, it was subjected to bakes in air. After a total heating time of 4 hours at temperatures up to 100°C, the low-temperature resistivity was 1.0×10^{7} ohm·cm. It would appear that two types of change can occur upon heating, depending upon the ambient, and that both can lead to an increase of resistivity.

The dependence of dark current upon electric field for film S7B in its high-resistivity condition is shown in Fig. 11 for fields up to about 10^{3} V/cm. The data points for both polarities of applied voltage demonstrate that there is no significant asymmetry with direction of current flow. The sample is ohmic for fields up to about 350 V/cm. At higher fields there is a small negative deviation from linearity. Some films have shown positive deviations at high fields.

The photoconductive response, as a function of bias voltage, of film S7B to 500°K blackbody radiation is given in Fig. 12. The conditions of measurement were

Sample temperature	129°K
Sample resistance	$\sim10^{8}$ ohms
Load resistance	1×10^{6} ohms
Radiation flux on sample	2.9×10^{-7} W
Chopping frequency	90 Hz

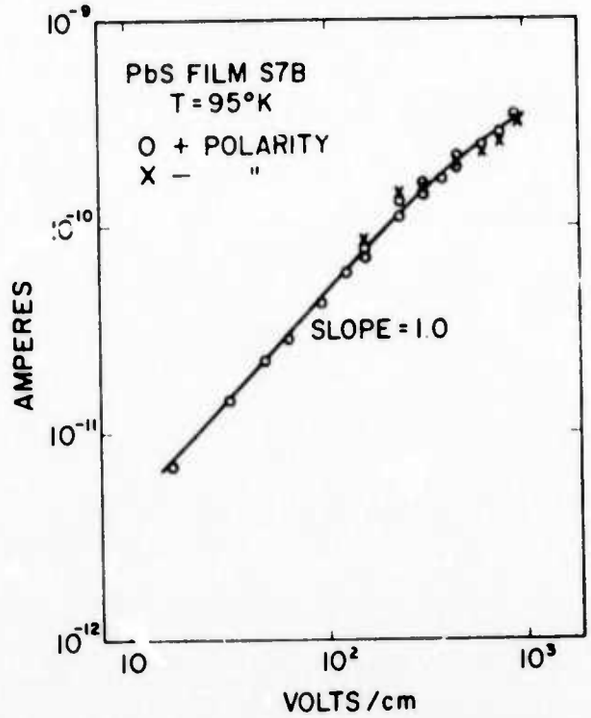


Figure 11. Dependence of dark current upon electric field for PbS film S7B.

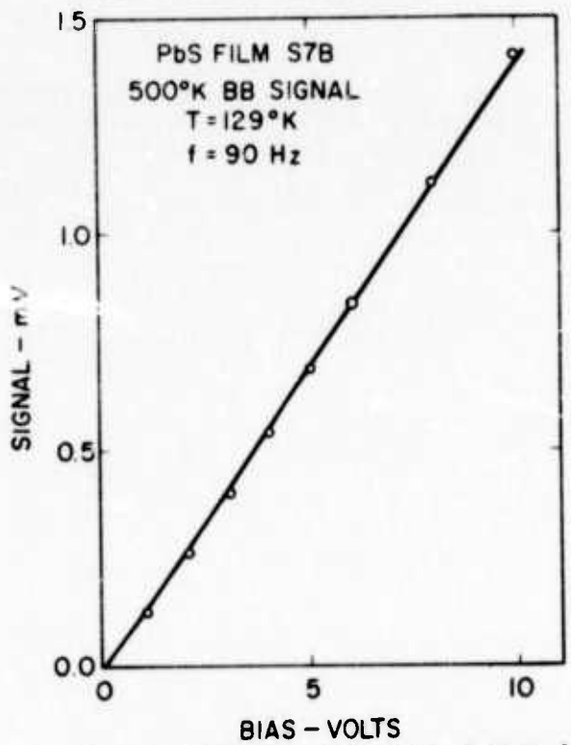


Figure 12. Photoconductive response of PbS film S7B to 500°K blackbody radiation as a function of bias voltage.

The signal voltage is proportional to bias voltage. It should be noted that the sample resistance is lower than would correspond to dark resistivity values given earlier. This difference is due to insufficient shielding of the sample from stray dc radiation in the photoconductivity measurements.

The absolute spectral responsivity, computed from the blackbody responsivity and the relative spectral response and expressed as $\Delta\sigma$ per watt of incident radiation, for each of the three samples discussed in this section, is given in Fig. 13. The curves seem to be made up of several incompletely resolved peaks which appear with different prominence for different samples. The curves do not resemble that to be expected for a simple, constant quantum efficiency photoconductor. For the three curves, the spread in absolute responsivity over most of the wavelength range is less than a factor of about five. The wavelength range of useful response extends to slightly beyond 3 μm.

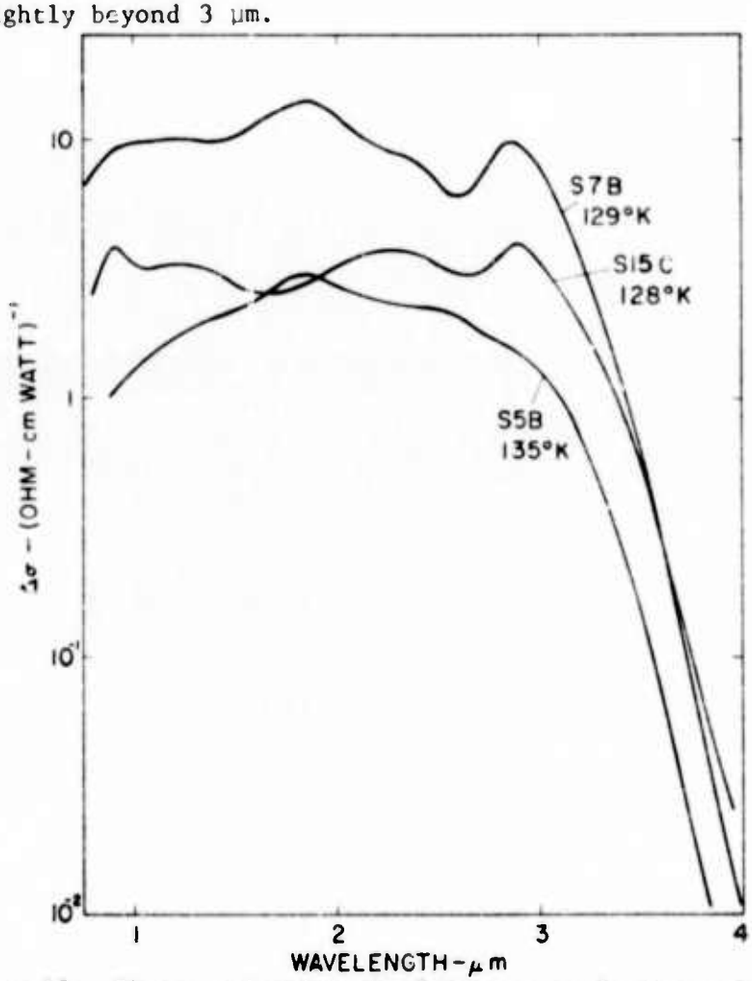


Figure 13. Photoconductive absolute spectral responsivity curves for PbS films S5B, S7B, and S15C.

E. DELINEATION OF PbS PHOTOCONDUCTIVE FILMS

The results summarized in the preceding section demonstrate that although there are a number of unanswered questions concerning the behavior of high-resistivity PbS, this material has properties which make it potentially useful as the radiation-sensitive material for the charge-coupled scanned IR imaging sensor. In order to fabricate this device it is necessary to be able to delineate, by photoresist masking and etching techniques, PbS elements of appropriate size and density. Once such a delineation process has been devised, it is necessary to show that the electrical properties of the PbS so delineated still satisfy the device requirements. The investigation of this group of problems has been commenced.

In the first attempts to delineate a PbS film, a Shipley photoresist pattern was applied to the surface of an SiO_2 layer on Si. A PbS film was then deposited over the pattern. Attempts to remove the overlying PbS selectively by dissolving the underlying photoresist were unsuccessful. Evidently, the PbS film protected the photoresist from attack by the solvent.

The order of the application of the photoresist and the PbS was reversed in the next attempts. PbS was deposited everywhere over the SiO_2 and then a Shipley photoresist pattern was applied over the PbS film. An etch consisting of dilute HCl-NH_4Cl solution removed the PbS not protected by photoresist without attack of the protected PbS. Finally, the photoresist was removed with solvent.

Properties of the first sample prepared in this manner, S18A2, are being determined. The sample initially had a resistivity of 16 ohm·cm at room temperature and 3.5×10^2 ohm·cm at 100°K. After a 3-hour vacuum anneal at 100°C, the corresponding values were 9 ohm·cm and 46 ohm·cm. The change in resistivities which occurred is in the opposite direction from that observed in all of the previous vacuum-annealing treatments. Contact of the PbS with photoresist has produced a significant change in the annealing behavior.

After this result had been obtained, the effect of low-temperature heat treatment in air was determined. After a total of 8 hours of heating at temperatures up to 100°C, the low-temperature resistivity had increased only to 6×10^2 ohm·cm. A similar heat treatment of sample S5B for half

the time had yielded a resistivity of 10^7 ohm·cm. Again, there seems to be a significant effect of the contact of the PbS with photoresist.

Next, heat treatment of film S18A2 in air for long times at somewhat higher temperatures was carried out. The results obtained are summarized in Table 2. A resistivity nearly large enough to satisfy the device requirement has been reached after a long time of heating. The trend shown by the results strongly suggests that still higher values of resistivity will be obtainable with further heating.

Table 2 - Heat Treatment in Air of PbS Film S18A2

Temperature (°C)	Time (hr)	ρ at 300°K(ohm·cm)	ρ at 100°K(ohm·cm)
111	8	7.2×10^1	2.6×10^3
122	7½	1.8×10^2	8.8×10^4
125	6½	3.0×10^2	1.0×10^6

It is known that excessive oxidation of PbS films results in loss of responsivity at wavelengths near the PbS peak and in enhancement of responsivity at wavelengths near 1 μm. These changes are believed to be due to the conversion of PbS to PbO or to other Pb-O compounds. Determination of the absolute spectral responsivity of PbS film S18A2 has shown that this has not occurred to any great extent as a result of the prolonged oxidation treatment given. Response curves for this sample are given in Fig. 14. Curves 1 and 2 give results of measurements made at a sample temperature of approximately 130°K. Curve 3 gives the response at room temperature. Curve 1 was obtained before the series of long heat treatments listed in Table 2 was carried out. Curve 2 was obtained after the completion of this series. The additional oxidation has resulted in a decrease of responsivity but by no more than a factor of two. There has been a slight development of a peak near 1 μm.

Curve 4 of Fig. 14, for sample S7B, is taken from Fig. 13 and is given here for comparison. The responsivity of S18A2, even in its most highly oxidized state, is substantially higher than that of the earlier samples.

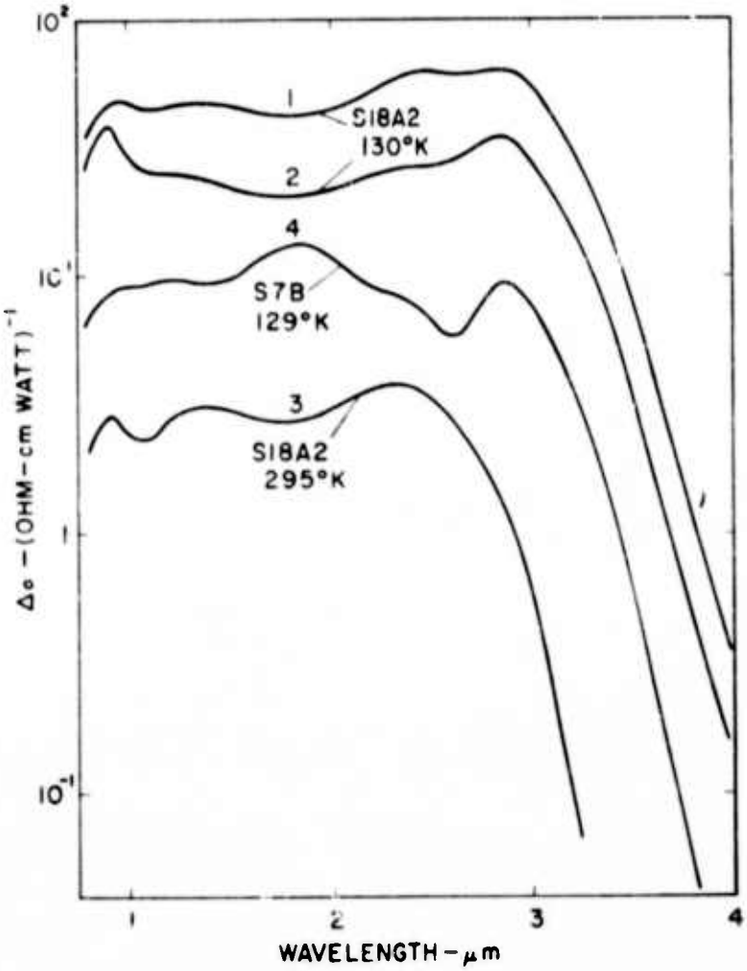


Figure 14. Photoconductive absolute spectral responsivity curves for PbS films S7B and S18A2.

The improvement at wavelengths larger than 2 μm is especially striking and is higher by up to an order of magnitude. This difference in responsivity may be associated with the difference in heat treatment behavior or it may be coincidental. This cannot be decided on the basis of the behavior of one sample.

Curve 3 of Fig. 14, taken at room temperature, is for the same state of oxidation of sample S18A2 as that for Curve 2. The peak responsivity has increased by over an order of magnitude upon cooling. The magnitude of the shift of the long-wavelength photoconductive edge to longer wavelength upon cooling gives a temperature coefficient of approximately 4×10^{-4} eV/°K. This value agrees satisfactorily with that of the temperature coefficient of the energy gap of PbS, 4.5×10^{-4} eV/°K [7].

F. LEAD SULFIDE-SILICON HETEROJUNCTIONS

The preparation of PbS-Si heterojunctions by chemical deposition of PbS upon n-type Si has been described [13]. The I-V characteristics at room temperature were given and showed marked rectification characteristics. The forward direction of current flow occurred with the PbS biased positive consistent with a p-type PbS layer. The reverse current was on the order of several microamperes for a bias of 1 V. No I-V characteristics for reduced temperatures were given. Photovoltaic response was observed at wavelengths corresponding to excitation of carriers both in the Si and in the PbS. If such heterojunctions had sufficiently small reverse bias dark currents at reduced temperatures, they could serve as the radiation-sensitive elements of the imaging device.

In order to investigate this possibility, a heterojunction, sample S16B, was prepared by chemical deposition of a PbS film on nominally 5 to 10 ohm·cm n-type <100> Si. The film area was 0.25 cm^2 and its thickness was 0.33 μm. Electrical contact to the PbS film was made by a small Ag paste dot. The sample was mounted in the glass dewar in the usual manner. The I-V characteristics were measured point by point. Great care had to be taken to shield the sample from stray radiation since the photoeffects were large.

Some of the I-V dark characteristics obtained are shown in Fig. 15 for room temperature and in Fig. 16 for low temperature. Note that the voltage and current density scales differ for the forward and reverse directions. The sign of the voltage gives the polarity of the PbS relative to the Si. Curves labeled 1 refer to the sample in the as-prepared condition. Diode behavior is clearly indicated. The forward direction occurs with the PbS layer biased positive. This indicates, as expected, that the PbS layer is p-type. The reverse bias current density at room temperature is about 2×10^{-5} A/cm^2. At 135°K it is on the order of 1 to 2×10^{-10} A/cm^2. Breakdown is gradual and occurs in the 5 to 10 V range. The small magnitude of the reverse bias dark current when the sample was cooled definitely suggests the possibility of employing such a heterojunction as the radiation-sensitive element of the device.

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13. H. Sigmund and K. Berchtold, Phys. Stat. Sol. 20, 255 (1967). We are indebted to Prof. J. Zemel of the University of Pennsylvania for calling this work to our attention and valuable discussions.

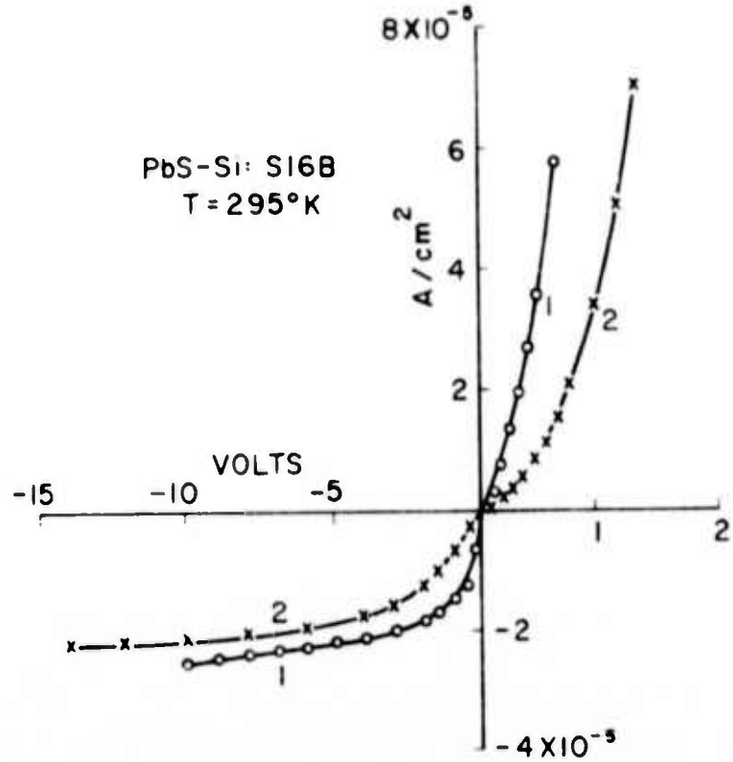

Figure 15. Current density/voltage characteristics of PbS-Si heterojunction S16B at room temperature.

The effect of vacuum annealing was investigated since the photoconductor films underwent large changes under such treatment. The sample was heated in vacuum for 3 hours at 92°C. This treatment resulted in a substantial reduction in the magnitude of the forward current but not much change initially in the reverse current. The I-V characteristics, remeasured after the sample had aged several days in vacuum at room temperature, are given as curves labeled 2 in Figs. 15 and 16. Of particular interest is the reverse bias curve for the cooled sample. The current density is 4×10^{-11} A/cm^2 or less for bias up to 8 V and is considerably less than it was originally. The breakdown is now much sharper than it was.

The reverse bias current of the aged, annealed sample was measured at several sample temperatures with a constant bias of 6 V applied. The thermal activation energy obtained from these data was 0.33 eV. This value is equal, within experimental error, to that found for the temperature dependence of resistivity of photoconductor samples. This result suggests

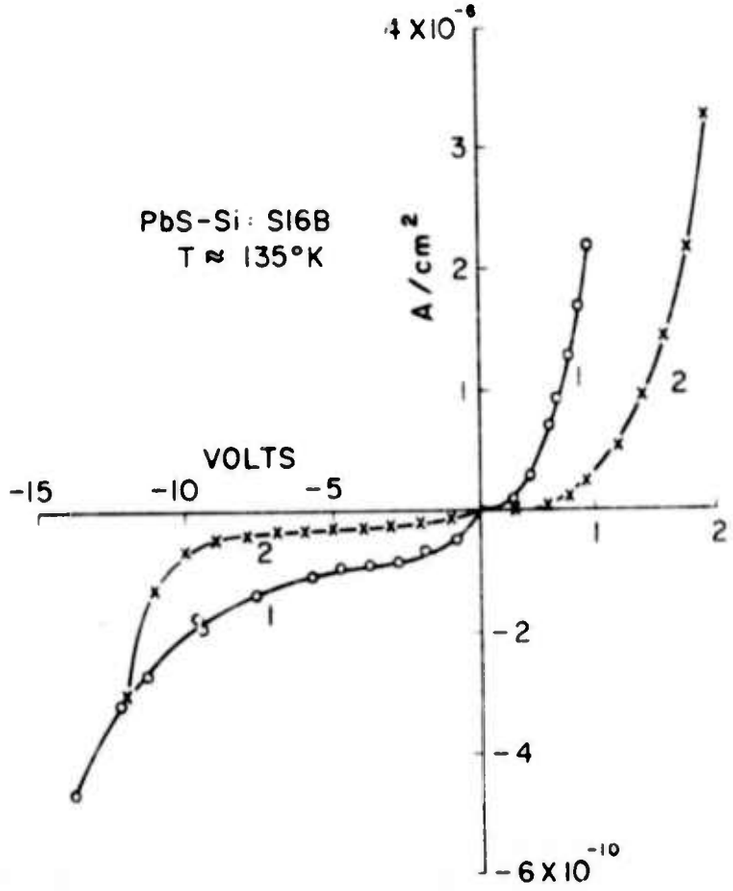

Figure 16. Current density/voltage characteristics of PbS-Si heterojunction S16B at reduced temperature.

that the principal cause of the reduction of the reverse bias current with decrease of temperature is the freezing out of carriers in the PbS.

The absolute photovoltaic spectral response of sample S16B, expressed as the short-circuit current in amperes per watt, is given in Fig. 17. The sample was irradiated from the PbS side. The absolute values are not very reliable because the 500°K blackbody signal was small and because it was very difficult to eliminate effects of stray radiation. The relative values, however, are reliable. Two points may be noted. (1) The PbS response is small compared with the Si response. This may be due to the small thickness of the PbS layer. (2) The response increases when the sample is cooled: by a factor of three for the Si peak and of twelve for the PbS. The signals increase, for both the Si and the PbS response, as negative bias is applied. Data at 1.0 and 2.0 μm for sample temperatures

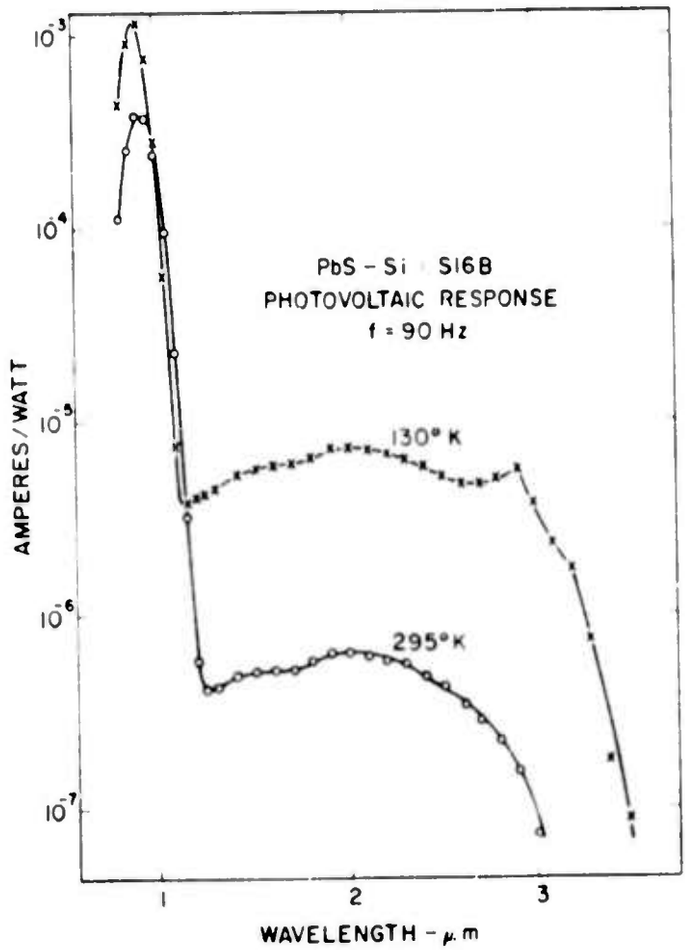

Figure 17. Photovoltaic absolute spectral responsivity curves of PbS-Si heterojunction S16B.

of 295°K and 130°K are given in Fig. 18. The behavior of the cooled sample at 2.0 μm is rather puzzling.

In order to obtain some estimate of the effect of the resistivity of the Si upon the properties of PbS-Si heterojunctions, a second sample, S18B, was prepared in a manner similar to that for S16B except that 0.1 ohm·cm n-type <100> Si was used. The PbS film was 0.38 μm thick. This sample was studied only in the unannealed condition. The sample showed essentially no rectification at room temperature. It did, however, exhibit photovoltaic response in both the Si and PbS wavelength regions. When the sample was cooled to 85°K, a rectification ratio of about six was observed. The I-V characteristic at this temperature is given in Fig. 19. The current density in the forward direction is roughly the same as that

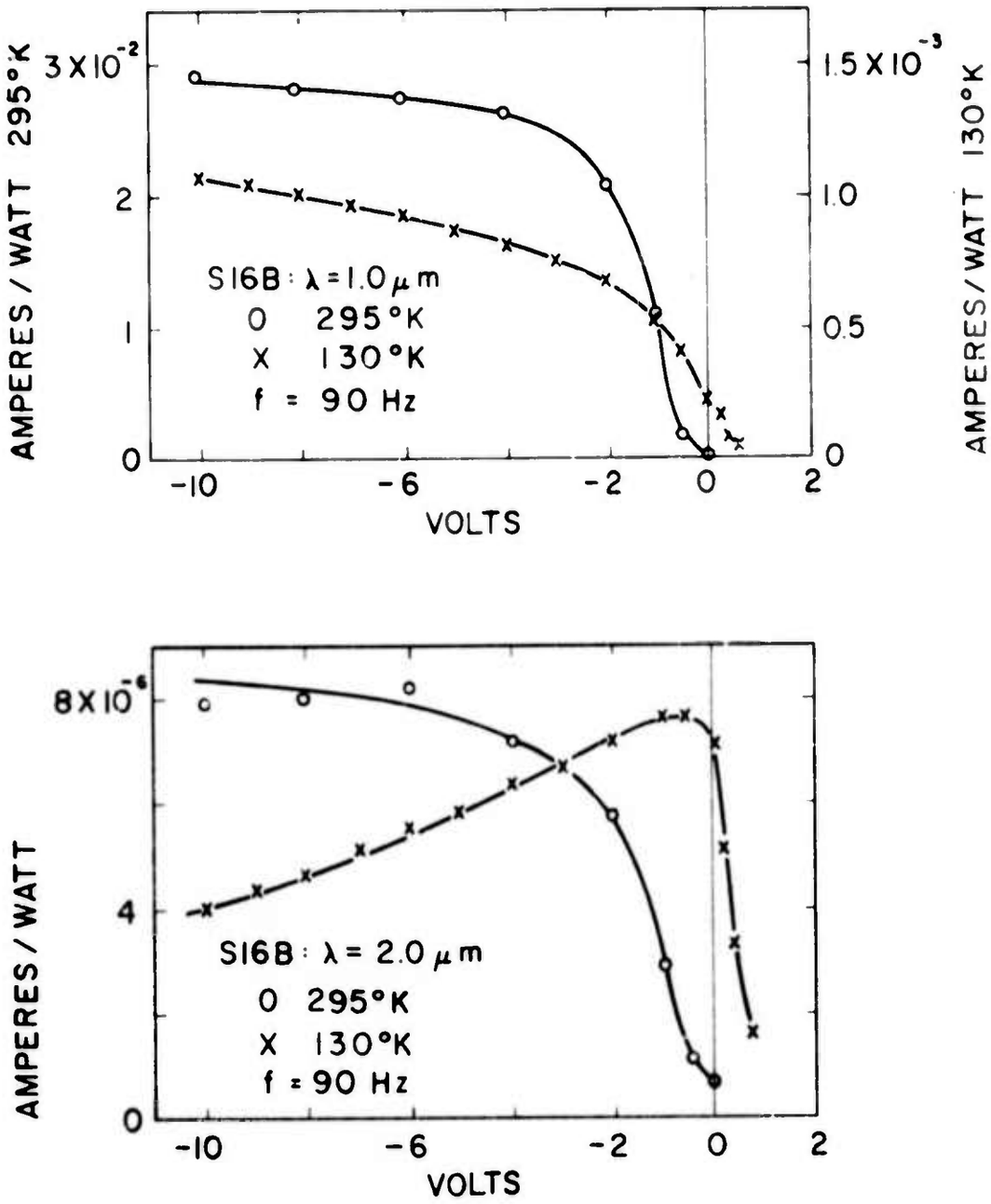

Figure 18. Dependence of absolute responsivity upon bias voltage for PbS-Si heterojunction S16B.

for S16B. That in the reverse direction is several orders of magnitude larger for S18B than for S16B.

Relative photovoltaic short-circuit spectral response curves for S18B at room temperature and at low temperature are given in Fig. 20. The photoresponse of this sample differs from that of S16B in two important

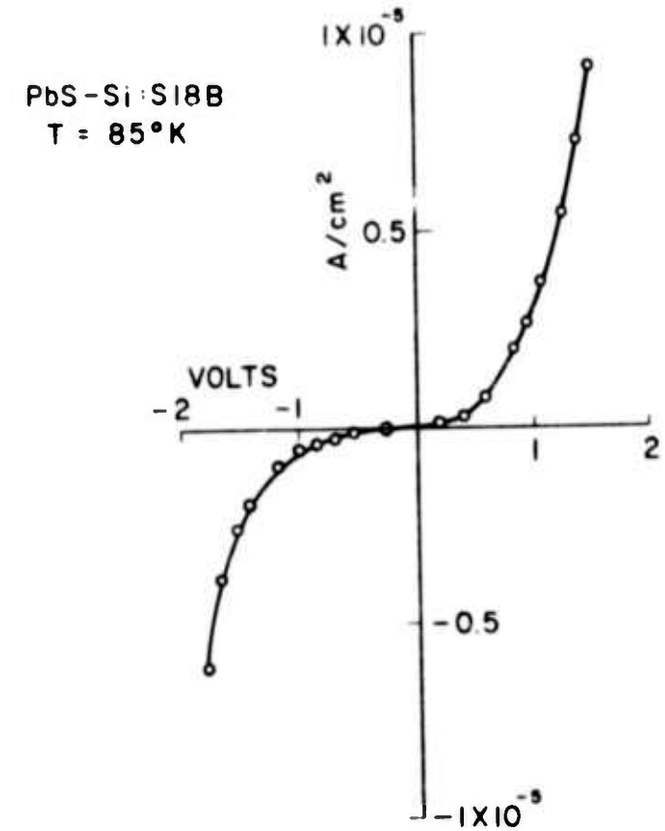

Figure 19. Current density/voltage characteristics of PbS-Si heterojunction S18B at 85°K.

respects: (1) The magnitude of the PbS response is comparable with that of Si. With S16B, the responses were very different. This difference in behavior of the two samples cannot be explained in terms of a difference in absorption since the PbS layer thicknesses were very nearly the same. (2) The responsivity of S18B was smaller at low temperatures than at room temperature. The opposite was true for S16B. The dependence of relative signal upon bias for 1.0 and 2.0 μm irradiation at room temperature and at 148°K is given in Fig. 21.

The substantial difference in the photoresponse behavior of the two PbS-Si heterojunction samples which have been studied indicates that additional investigation of the behavior of such structures is necessary in order that their evaluation as sensors for the imaging device be placed on a firm foundation. In particular, the behavior of heterojunctions made with Si of resistivity intermediate between 0.1 and 10 ohm·cm must be determined.

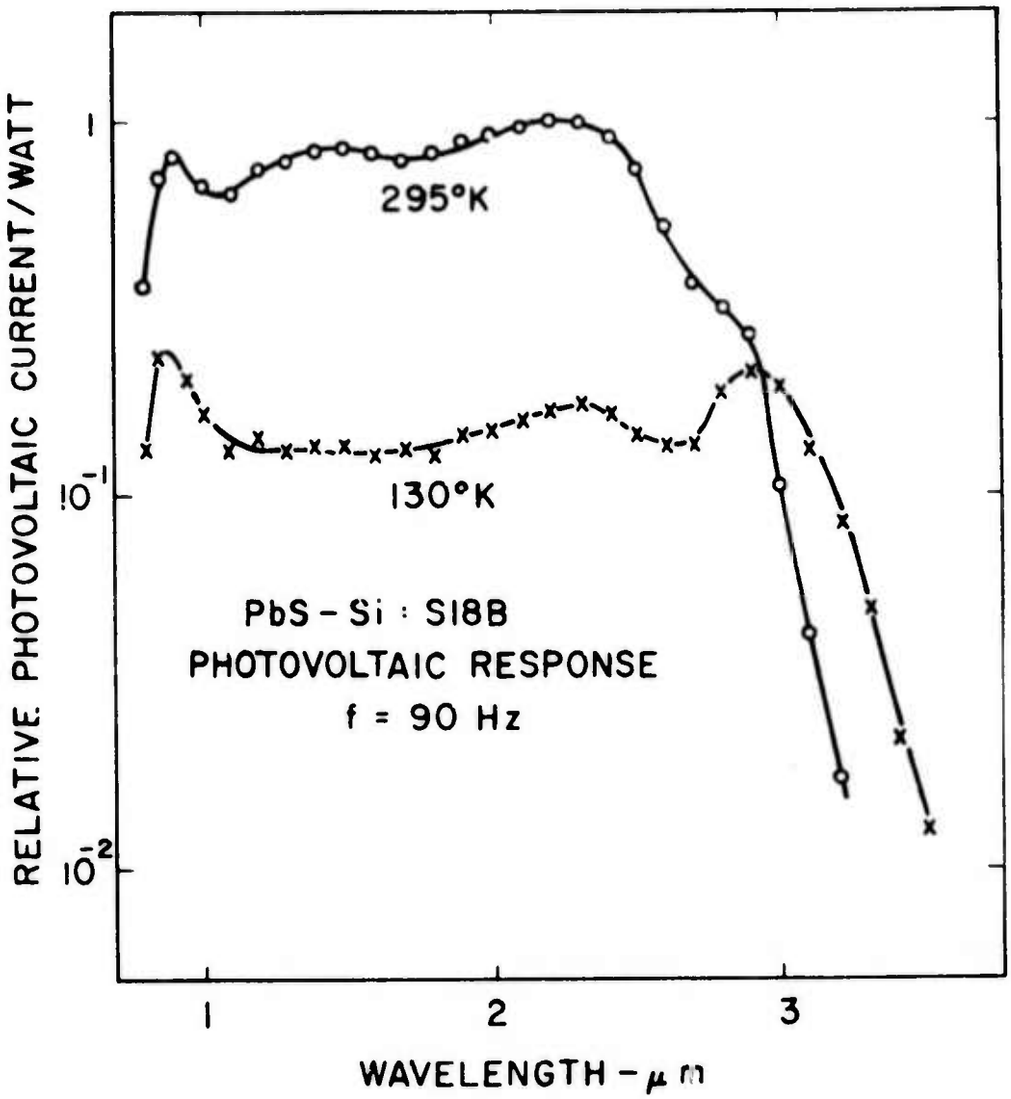

Figure 20. Photovoltaic relative spectral responsivity curves of PbS-Si heterojunction S18B.

It is also necessary to investigate the behavior of heterojunctions delineated by photoresist masking in view of the differences in behavior of photoconductor films which have been so delineated.

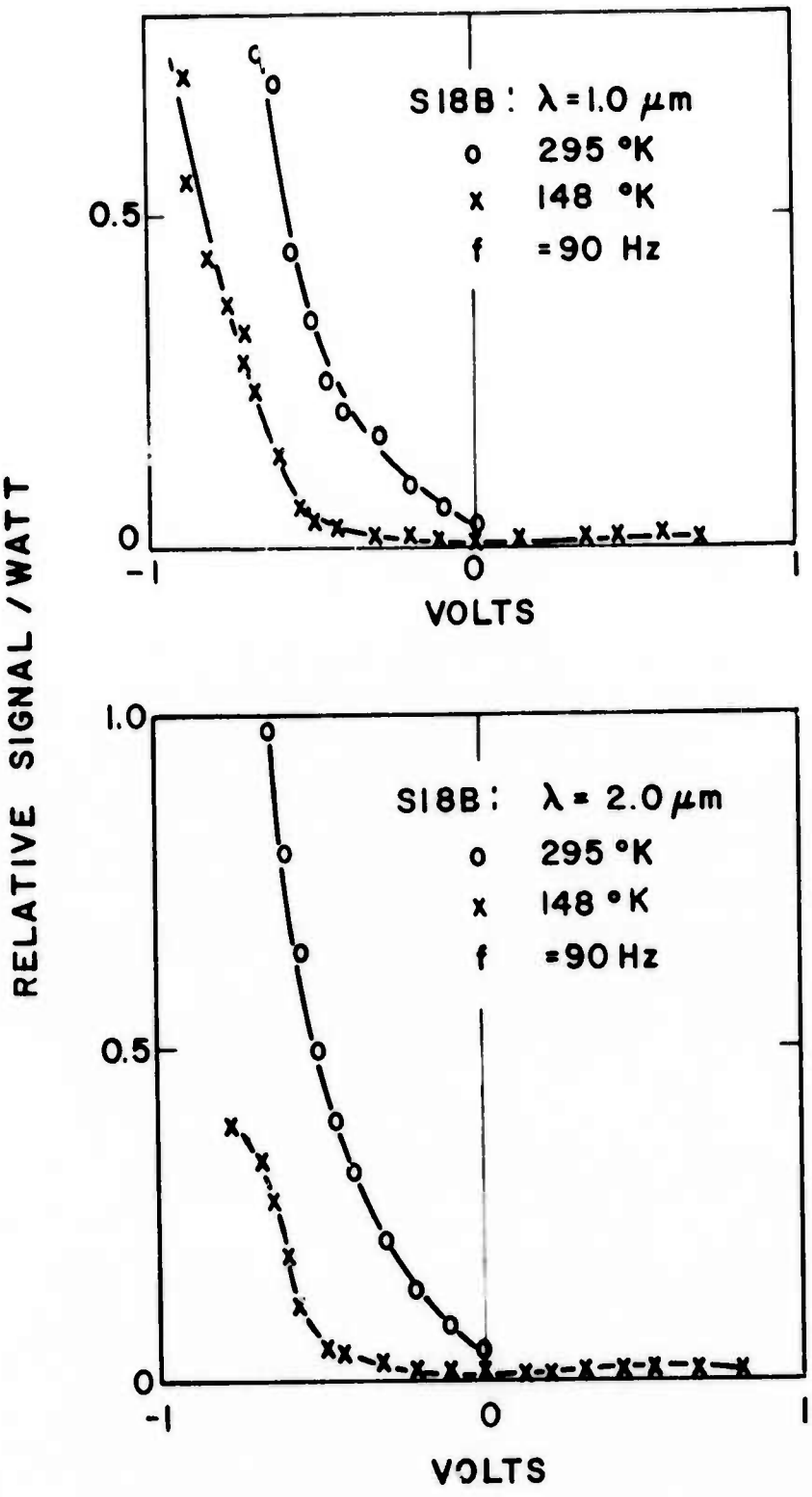

Figure 21. Dependence of relative responsivity upon bias voltage for PbS-Si heterojunction S18B.

X. LEAD TELLURIDE

Epitaxial and polycrystalline films of IV-VI compounds have been studied extensively for their photoconductive properties [8,14-20], and recently rf-sputtered ternary chalcogenides have shown interesting properties [20]. We used an rf-sputtering technique to deposit PbTe polycrystalline photoconductive detectors and to obtain responsivity and detectivity values higher than previously reported. One objective of this work was the determination of whether or not films of this material, having resistivities large enough to satisfy the imaging device requirement, could be prepared by sputtering.

A diode rf-sputtering system with a liquid-nitrogen baffled oil-diffusion pump was used. The target was a 5-inch PbTe layer of $4N^{+}$ pressed powder. The ultimate vacuum before sputtering was 6×10^{-8} torr and a pre-sputtering of at least 60 min was used to clean the target surface of adsorbed atmospheric impurities.

The films were deposited onto glass or silicon substrates heated up to 320°C. Three basic methods were used to introduce oxygen into the films. The first method was based on sputtering a surface-oxidized PbTe target in an argon atmosphere. In the second method, pulses of oxygen at a pressure of 20 μ Hg were admitted intermittently into the system while the sputtering was interrupted. The third technique consisted of reactive sputtering of PbTe in a 10% O_2 90% Ar mixture. Deposition rates close to $\sim$ 2 Å/sec and sputtering pressures of less than 10 μ Hg were normally used. Film thicknesses usually ranged between 1 and 3 μm.

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The crystallite size in PbS and PbSe film detectors generally falls within the range between 10^3 and 10^4 Å [21]. The sputtered PbTe films had comparable grain sizes. Significant differences were found in grain size, texture, and crystalline orientation of the films depending upon the sputtering conditions. Lead oxide phases were found in films deposited by oxygen reactive sputtering; higher preferential ordering in crystallinity seems to be associated with a (100) orientation typical of this deposition. The reactively sputtered polycrystalline films had a grain size smaller than those activated by intermittent admission of oxygen. Ohmic contacts at bias currents from 10^{-9} to 5×10^{-6} A were obtained at 77°K operating temperature by evaporating Au electrodes on the substrates prior to the deposition of the PbTe films.

We have found that films deposited by methods 2 and 3 were very stable, while films deposited by method 1 have shown noticeable change in resistivity upon exposure to air. Thus, while the terminal resistivity vs. temperature was nearly identical for all three types of films after several days of exposure to air (Fig. 22), the initial resistivity values of films prepared by method 1 were much lower. All three types of films showed almost no further change in resistivity after being exposed to alternate vacuum and air exposure cycles, unlike previously reported lead salt polycrystalline films. The thermal activation energy for dark resistivity of the stabilized films was 0.15 eV over the temperature range from 300°K to about 160°K and was about 0.06 eV at lower temperatures. The dark resistivities at 77°K have been about 5×10^4 ohm·cm. This value is too small to satisfy the dark-current requirement of the imaging device.

A comparison of the relative photoconductive performance of the three types of samples is given in Table 3. A typical relative responsivity curve, measured at 90°K for a sample prepared by the third method, is given in Fig. 23. Peak response occurs at 4.4 μm, and the threshold is near 5 μm. The highest absolute peak responsivity values have been in excess of 10^6 V/W for a bias current of 10^{-6} A. With the same bias, blackbody detectivities of 1.4×10^{10} cm $Hz^{1/2}/W$ and peak detectivities D* (λ_{peak},800,1) as high as 8.5×10^{10} cm $Hz^{1/2}/W$ have been measured with a 2 π steradians field of view.

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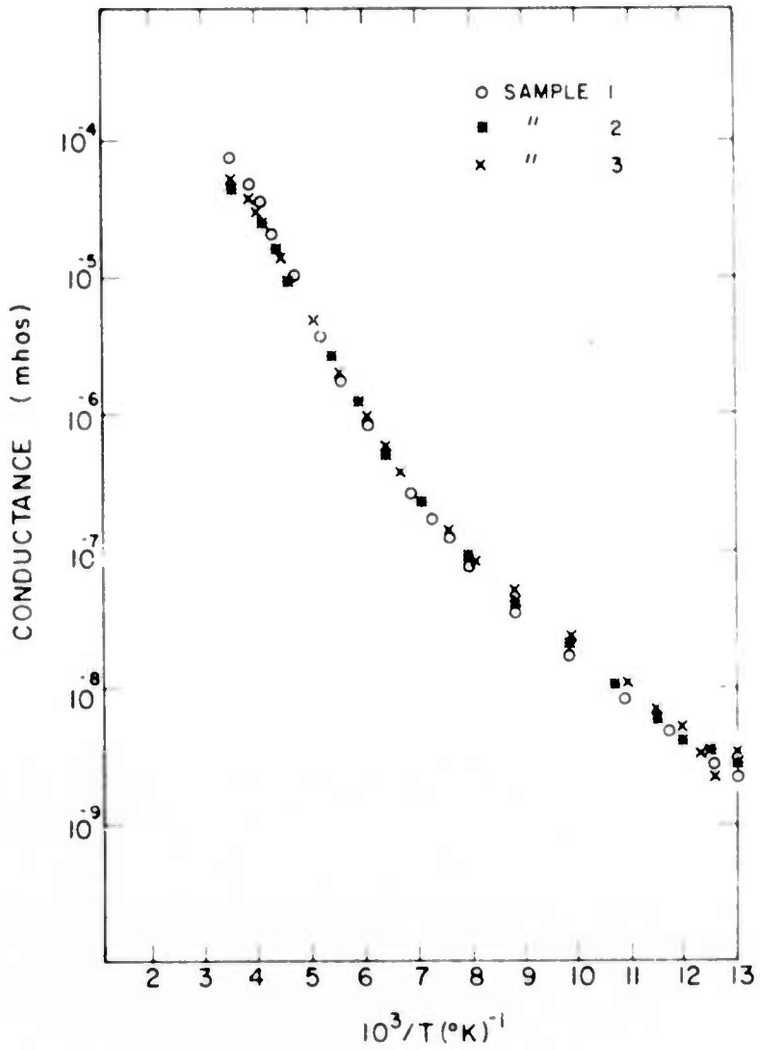


Figure 22. Temperature dependence of conductance of sputtered PbTe films after stabilization in air.

Table 3 - Typical Data for PbTe Film Detectors Sputtered by the Three Described Methods

Detectors (Deposition Method)	Resistivity (Arbitrary Units)	Responsivity (Arbitrary Units)	Blackbody Detectivity D* (500°K,800,1) (Arbitrary Units)
1	1.0	0.4	∿0.1
2	0.8	1.0	∿0.6
3	0.6	0.9	1.0

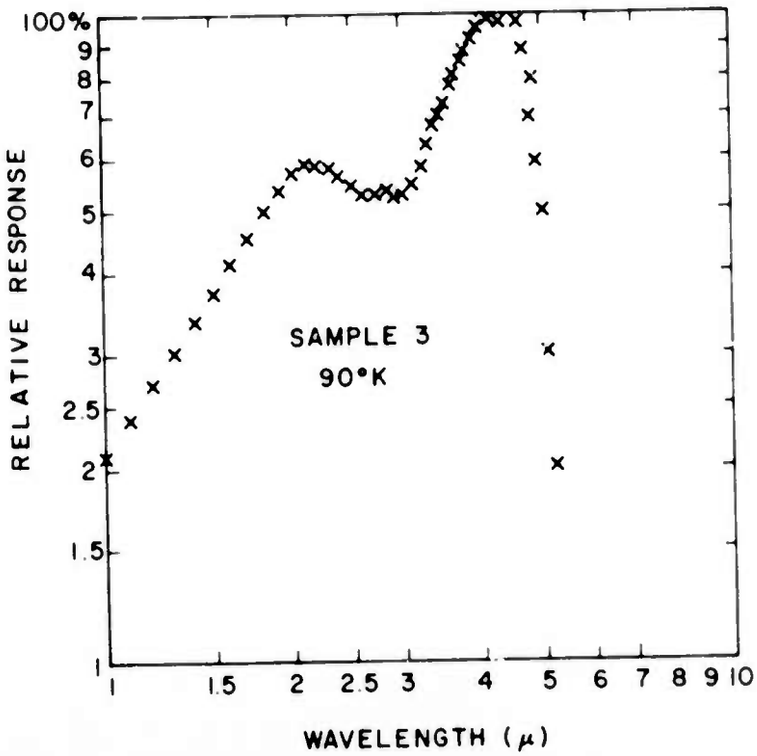


Figure 23. Relative spectral responsivity of a reactively sputtered PbTe film at 90°K.

A time constant in the ms range was measured in the spectral region close to 2.2-μm and 3.0-μm wavelength. However, the intrinsic photoconductor time constant as derived from noise measurements is of the order 10 to 30 μsec.

The present results show that rf-sputtered polycrystalline layers of PbTe can be used as middle infrared detectors with high responsivity and detectivity values. Easily deposited on wide substrate areas, the oxygen reactive-sputtered PbTe detectors show stabilities much better than previously reported polycrystalline films. The highest dark resistivities attained thus far by this method of preparation of PbTe films are about two orders of magnitude lower than the minimum value required for the device.

APPENDIX A

IR-CCD DRIVER CIRCUITRY

The basic three-phase CCD requires three waveforms consisting of slightly overlapping pulse trains. Thus, each pulse train has a duty cycle just over one third. These basic waveforms can be generated by a pair of J-K flip-flops as shown in Fig. A-1. When data inputs J and K are connected to a logical "1", a J-K flip-flop changes state (toggles) as the clock input goes from a "1" to a "0". Thus, a single J-K flip-flop can be used as a divide-by-two circuit, and a pair in cascade divides by four. In our circuit, a NAND gate samples the outputs and resets (clears) both flip-flops at a count of three, yielding the waveforms shown for Q_1 and Q_2. The third waveform is generated from the first two with a NOR gate. When the first two waveforms go to "0", the third goes to "1". There are spikes present in the first waveform, Q_1, halfway between the pulses. These spikes are essential to the logical operation of the circuit and can be filtered out only after buffering the output. The basic clock waveform is generated by a separate astable multivibrator. Its frequency determines the CCD bit rate and can be varied without changing the relationship between the waveforms. The clock waveform in Fig. A-1 need not be symmetrical, since only the fall of the clock affects this circuit. Indeed, there is a reason for making it unsymmetrical, namely, to generate overlap. Figure A-2 shows the overlap-generating circuit. The clock waveform is the same one as in Fig. A-1, but it is drawn to have a duty cycle greater than 50%. One of the three-phase waveforms, Ø, is shown making its transitions on the fall of the clock as before. The type "D" flip-flop has a single data input D. The output simply takes on the value of the input on the rise of the clock and holds it until the next rise of the clock. Thus, the output Ø' of our D flip-flop is just the input Ø delayed by the time the clock is at "0". The input Ø and the output Ø' are put through an "OR" gate to generated Ø", the stretched pulse train. Since its duty cycle is greater than one third, it will overlap the beginning of the pulse applied to the next phase as required.

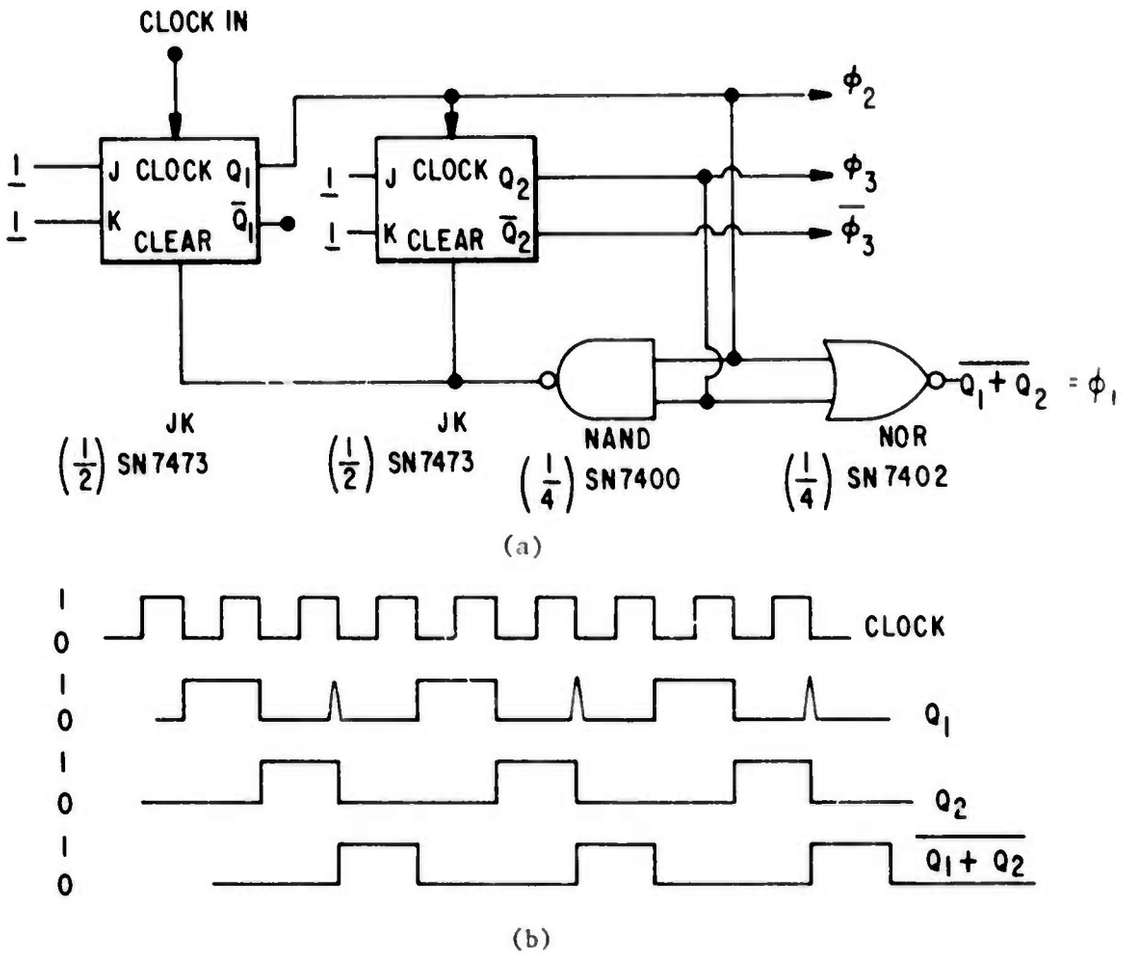


Figure A-1. The 3-phase generator. The J-K flip-flops have their data inputs set to logical "1" so that they change state each time the clock falls. The three output waveforms are shown in synchronism with the clock waveform.

The Schottky-barrier IR-CCD requires a setting pulse and a transfer pulse as well as the three phases. The relationship between these auxiliary pulses is shown in Fig. A-3. A frame trigger pulse initiates the sequence that includes a setting pulse, a delay which is the integration time, and a transfer pulse. Each must begin as the previous one ends. All three delay times must be continuously adjustable, and the two pulse heights must be adjustable separately from the height of the three-phase pulse trains. Furthermore, while the transfer pulse is on, the three-phase pulse trains must stop with phase 1 high and phases 2 and 3 low to permit

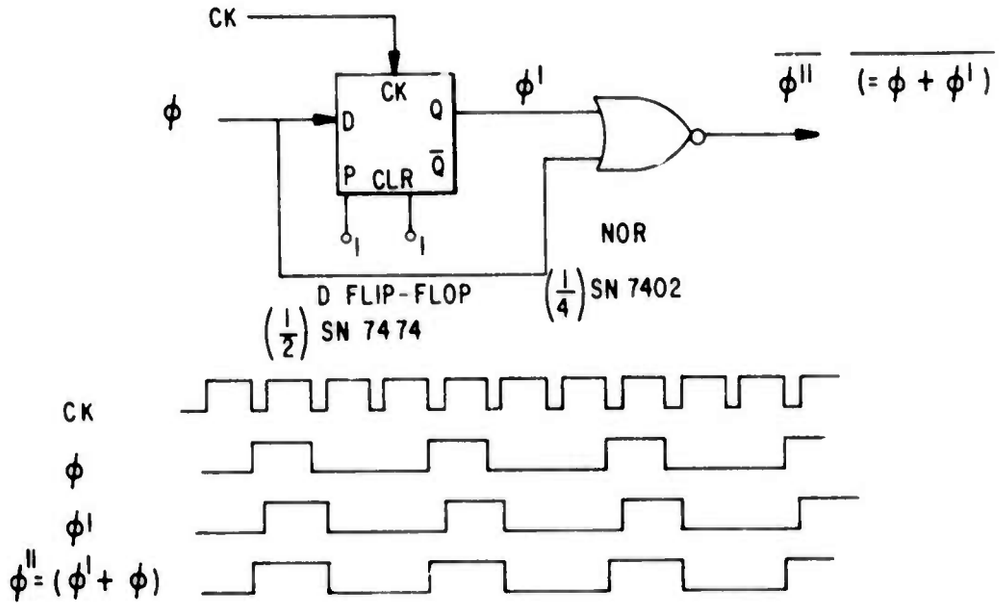


Figure A-2. The pulse-overlap circuit. The output of a D flip-flop Q takes on the value of the data D on the rise of the clock and holds it until the next time the clock rises. Thus, the pulse is stretched by the length of the clock off-time.

loading. The auxiliary pulses are generated by three monostable flip-flops triggering each other in sequence as shown in Fig. A-3. Additional logic, however, is required to make the pulse trains stop at the proper time when the transfer pulse goes on. This is necessary because the clock is not synchronized to the flip-flops. If the transfer pulse were to stop the clock directly, phase one ($\emptyset_1$) would not necessarily be high. The circuit must therefore cause the clock to stop after the transfer pulse begins but not until the next time $\emptyset_1$ comes on. The actual application of the transfer pulse to the amplifier must be delayed until this condition has been met.

In Fig. A-4, the first "D" flip-flop delays the raw transfer pulse A until phase three drops ($\overline{\emptyset}_3$ rises). This happens to be when $\emptyset_1$ rises (see Fig. A-5 for the timing diagrams). It is followed by an "AND" gate to verify that the transfer pulse is still on. The delayed transfer pulse B is delayed again by the second "D" flip-flop until the clock rises again half a cycle later, yielding waveform C, the timed transfer pulse. This waveform is combined with the clock itself in the "OR" gate, yielding the gated clock that actually runs the three-phase generator shown in Fig. A-1.

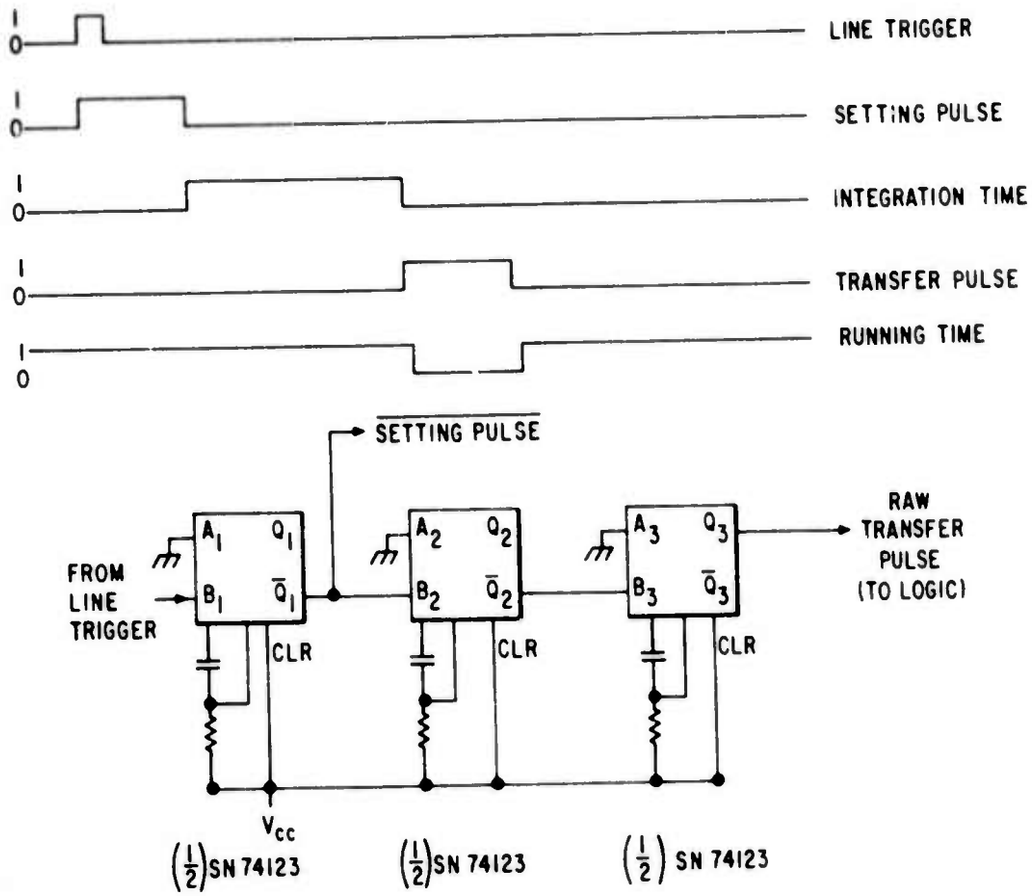
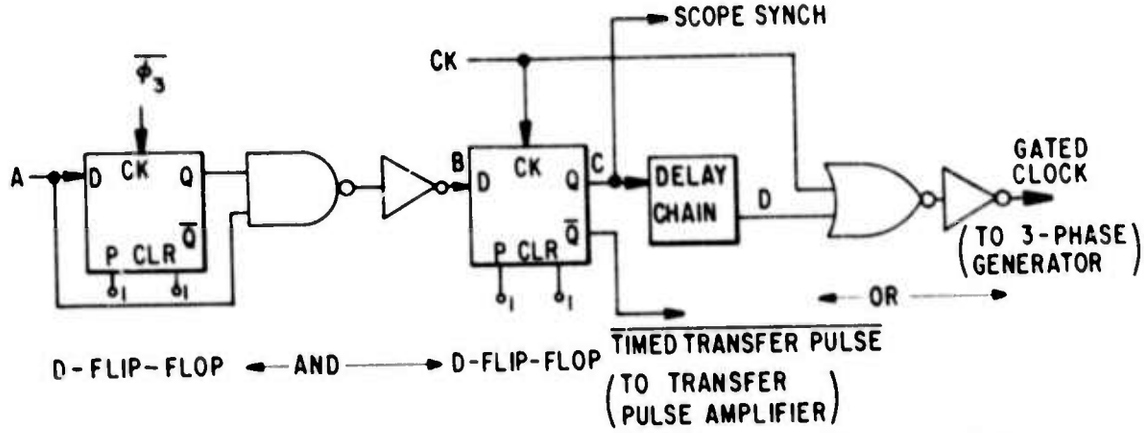


Figure A-3. Timing diagram for the auxiliary pulses. The one-shot flip-flops trigger each other as shown and produce the setting pulse and the raw transfer pulse. The "running time" curve indicates when the 3-phase generator is running.

Note that once the timed transfer pulse begins, the gated-clock remains high. The three-phase generator in Fig. A-1 remains with $\emptyset_1$ on and $\emptyset_2$ and $\emptyset_3$ off as required to load information into $\emptyset_1$. When the raw transfer pulse A ends, the delayed transfer pulse B ends immediately because of the AND gate. The next time the master clock pulse rises, the timed transfer pulse ends. When the master clock pulse falls, the gated clock also falls, thus transferring the signal charges from $\emptyset_1$ to $\emptyset_2$, and beginning the CCD readout. When the timed transfer pulse ended as the master clock rose, there is a possibility that the output of the OR gate could go to zero momentarily, causing improper operation (Note 4 in Fig. A-5).



$\left(\frac{1}{2}\right)$ SN 7474, $\left(\frac{1}{4}\right)$ SN7400, $\left(\frac{1}{6}\right)$ SN7404, $\left(\frac{1}{2}\right)$ SN 7474, $\left(\frac{4}{6}\right)$SN7404, $\left(\frac{1}{4}\right)$ SN7402, $\left(\frac{1}{6}\right)$ SN7404,

Figure A-4. The clock-gating circuit. This circuit is required to ensure that the clock will stop with $\emptyset_1$ on after the transfer pulse begins. It also provides the timed transfer pulse and the scope trigger.

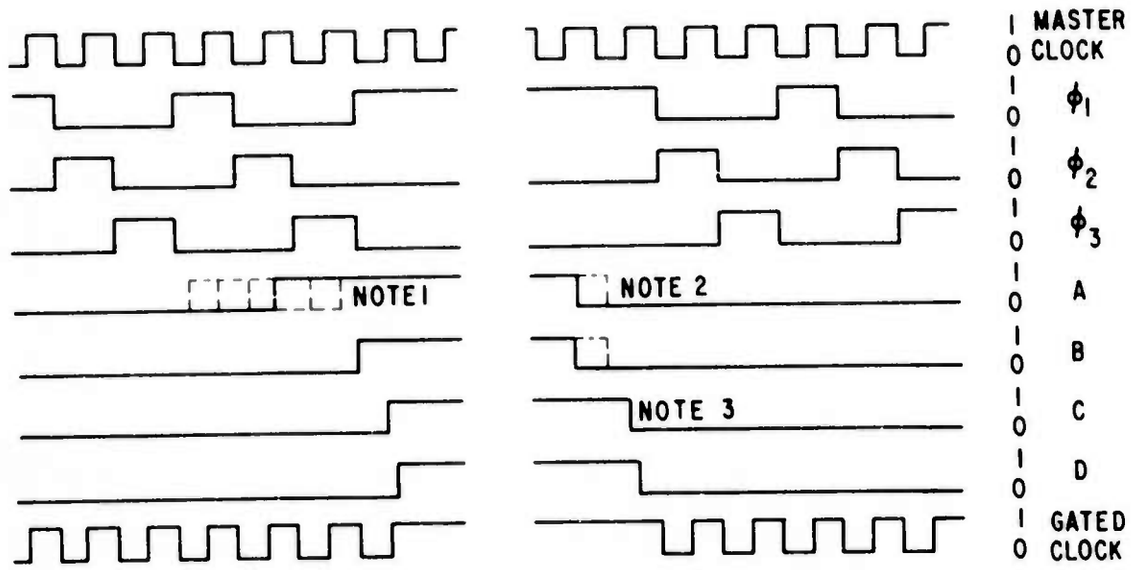


Figure A-5. Timing diagram illustrating the operation of the clock-gating circuit shown in Fig. A-4. The notes are explained in the text.

To prevent this from happening, a delay chain consisting of an even number (4) of inverter stages in cascade is included in the path. Thus, the timed transfer pulse, as seen by the OR gate, does not end until a measurable time after the clock connected to its other input has gone high. The delay is of no consequence when the timed transfer pulse rises because the clock is already high at that time.

Since the delays generated by the one-shot flip-flops are not multiples of the clock period, the raw transfer pulse could rise while the three-phase generator is in any one of six logical conditions, namely any one of the three phases on with the clock up or down. An inspection of Fig. A-5 (Note 1) shows that the subsequent operation is as previously described, regardless of when the raw transfer pulse begins. This is because nothing happens until the next time $\emptyset_3$ drops. Similarly, the raw transfer pulse can end with the master clock up or down (Note 2) although this time only $\emptyset_1$ can be high. Again, it does not matter since the fall of the timed transfer pulse awaits the clock rise. The oscilloscope displaying the video signal can be triggered off the fall of waveform "C".

A block diagram of the system is shown in Fig. A-6. The master clock has adjustments for bit rate and overlap time, and it runs independently of the rest of the circuit. Similarly, the timing generator has the four adjustments shown, and it too runs independently, providing the raw transfer pulse to the clock gating circuit, and the setting pulse to a CCD gate driver. The clock gating circuit runs the 3-phase generator and provides the timed transfer pulse to its CCD gate driver. Also shown are the pulse stretchers and the CCD gate drivers. The CCD gate driver circuit, obtained from W. Pike of these Laboratories, is shown in Fig. A-7. It operates from TTL levels, and provides a pulse whose height is simply the supply voltage V_{CC}. The output can be offset by a bias source with the clamp circuit shown at the right of the output. While the system was designed for an n-channel CCD, it can be used for a p-channel device with only a modification of the gate-driver amplifier needed.

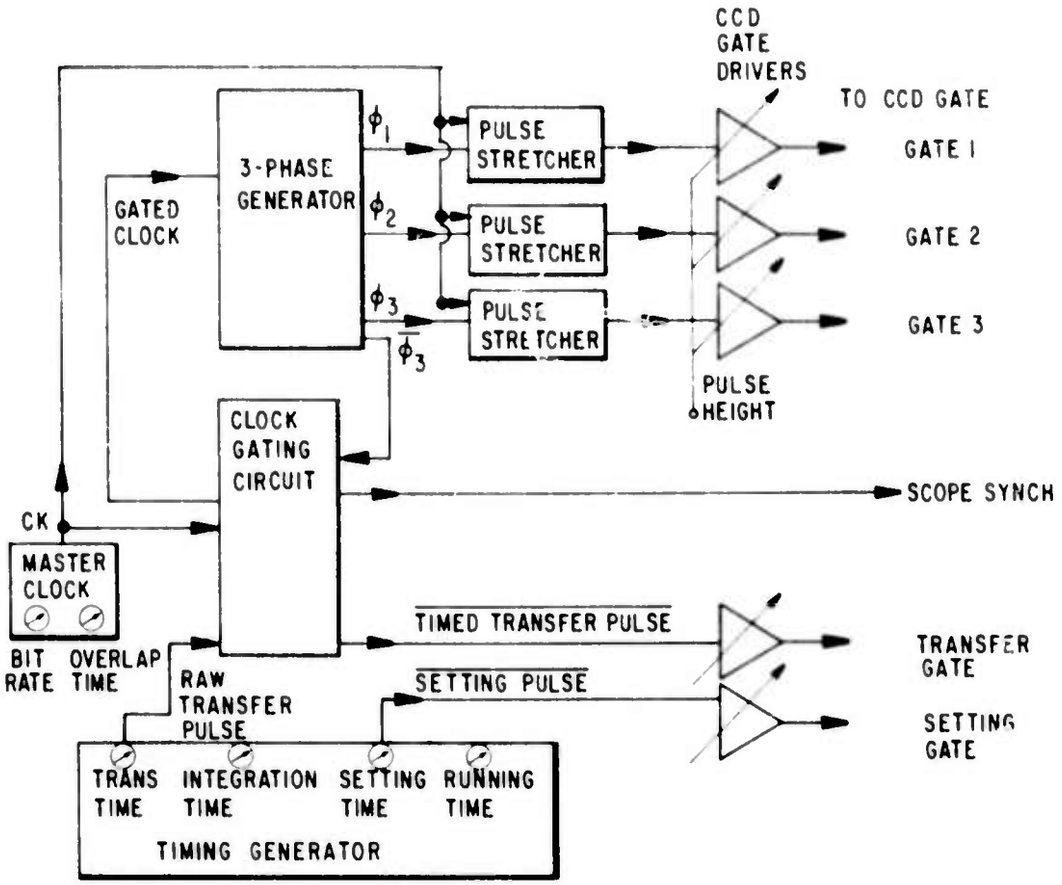


Figure A-6. Block diagram of the complete IR-CCD driver circuit.

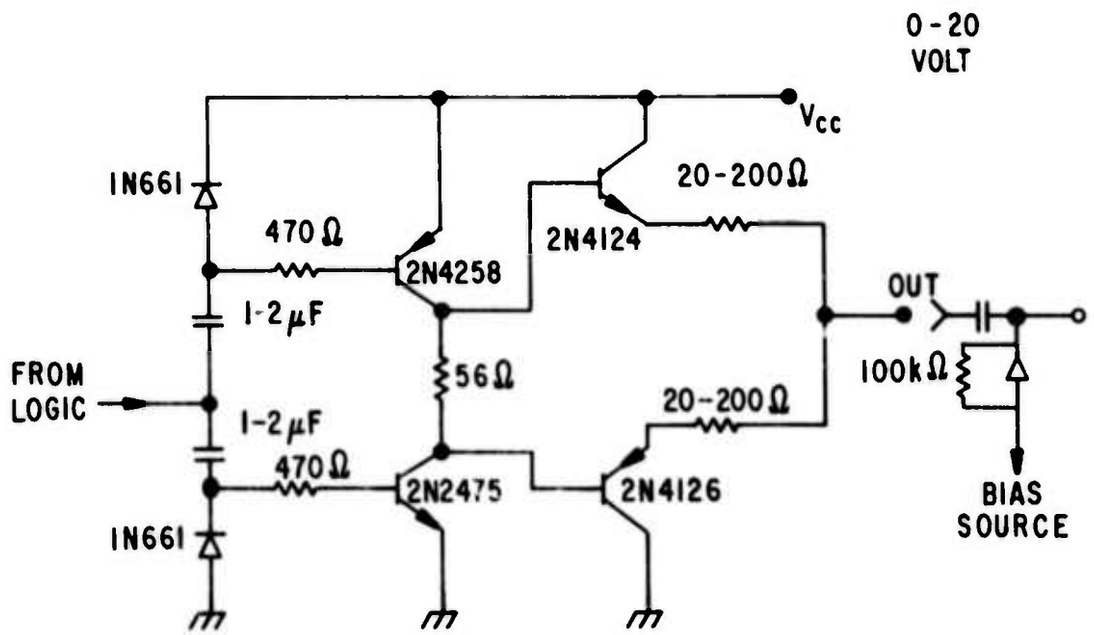


Figure A-7. Schematic diagram of a CCD gate driver.

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